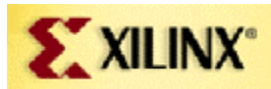
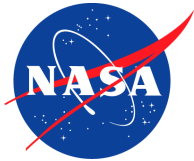


XILINX SINGLE EVENT EFFECTS

1ST CONSORTIUM REPORT

VIRTEX-II STATIC SEU CHARACTERIZATION



JANUARY 2004

EDITED BY

GARY M. SWIFT

JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY

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I. THE XILINX SEE CONSORTIUM

A. Introduction

The Jet Propulsion Laboratory and Xilinx started the informal collaboration dubbed the Single Event Effects (SEE) Consortium or the Xilinx Radiation Test Consortium (XRTC) in 2002. Its purpose is to evaluate re-configurable FPGAs for aerospace applications. The SEE Consortium brings together experts from industry, government, and academia to characterize radiation effects and mitigation techniques for re-configurable FPGAs.

Radiation effects characterization for complex FPGAs such as Virtex-II and Virtex-II Pro is an expensive, complicated, and time-consuming endeavor. The members of the SEE Consortium have combined resources to provide more sophisticated and efficient experimentation and analysis.

Membership in the SEE Consortium is open to US organizations that have an interest in single event effects and SEE mitigation techniques for re-configurable FPGAs. The SEE Consortium publishes its results in periodic reports such as this one, which are publicly available.

This document is the first SEE Consortium Report; it details the experimental procedures, data, and conclusions of SEE Consortium's efforts to characterize single event effects in the Virtex-II Radiation Tolerant FPGA family.

Since its founding, the primary objective of the SEE consortium has been to collect in-beam data and to analyze radiation-induced upset and failure modes in the QPro Virtex-II Radiation Tolerant FPGA family. In cooperation with the Consortium's charter members, the Aerospace Corp., Sandia National Laboratories, SEAKR Engineering, Los Alamos National Laboratories, and ISI supported the work reported here. Testing activities were coordinated through the SEE Consortium to prevent redundant efforts and improve the breadth and quality of analysis.

SEE characterization radiation tests for Virtex-II divide into two general categories: static and dynamic. Static testing measures configuration memory upsets and Single Event Functional Interrupt (SEFI) failure modes in un-clocked design configurations. On the other hand, dynamic testing uses clocked designs and probes for additional upset sensitivities not observable in unswitched devices, mainly Single-Event Transient (SETs). This report describes the Virtex-II static upset test campaign and includes descriptions of the experimental setups, raw data, analysis, and results.

B. Xilinx SEE Consortium Members (in alphabetic order)

1) The Aerospace Corporation

El Segundo, CA, USA

Phone: (310) 336-2107

- Jeffrey George: jeffrey.s.george@aero.org
- Rocky Koga: rocky.koga@aero.org
- Robert Leatherman: Robert.H.L Leatherman@aero.org
- Richard LeBaron: Richard.K.Lebaron@aero.org
- John Maksymowicz: john.maksymowicz@aero.org
- Jon Swail: jon.swail@aero.org
- Thomas Tsubota: Thomas.K.Tsubota@aero.org
- Donald Yang: Donald.H.Yang@aero.org

Contribution:

- Provided heavy-ion beam time at Lawrence Berkeley Lab's 88" cyclotron
- Assisted with data acquisition and analysis
- Assisted with the static test vehicle design and preparation
- Aided in the development of the dynamic test methodology
- Published the test results at RADECS 2003: "Comparison of Xilinx Virtex-II FPGAs SEE Sensitivities to Protons and Heavy Ions," R. Koga, J. George, G. Swift, C. Yui, C. Carmichael, T. Langley, P. Murray, K. Lanes, M. Napier

2) Boeing Satellite Systems

P.O. Box 92919

Los Angeles, CA 90009

2260 E. Imperial Highway

El Segundo, CA 90245

Phone: (310) 335-6787

- Anthony Le: anthony.c.le@boeing.com
- George Madias: george.n.madias@boeing.com

Contribution:

- Took minutes at consortium meetings
- Assisted in setting up radiation testing experiments

3) *BYU University*

Brigham Young University (BYU)
Electrical and Computer Engineering
459 Clyde Building
Provo, UT 84602
Phone: (801) 422-7601

- Michael Wirthlin: wirthlin@ee.byu.edu

Contribution:

- Developed a system for injecting configuration faults in Virtex-I and Virtex-II devices

4) *Jet Propulsion Laboratory (JPL)*

Jet Propulsion Laboratory / California Institute of Technology
Radiation Effects Group, Electronic Parts Engineering Office
MS: 303-220, 4800 Oak Grove Dr.
Pasadena, CA 91109
Phone: (818) 354-5059

- Larry Edmonds: larry.edmonds@jpl.nasa.gov
- Gary Swift: gary.m.swift@jpl.nasa.gov
- Candice Yui: candice.yui@ngsc.com

Contribution:

- Provided Beam time at Texas A&M, UC Davis, and Indiana facility
- Development of the JPL/Xilinx 2V1K dynamic test board
- Participation in the development and the preparation of the test methodology
- Data acquisition and analysis
- Calculation of space-environment upset rates
- Publication of test results at MAPLD 2002 ("Single Event Upset Susceptibility Testing of the Xilinx *Virtex-II* FPGA," C. Yui, G. Swift and C. Carmichael, Poster Session) and NSREC 2003 ("SEU Mitigation Testing of Xilinx Virtex-II FPGAs," Candice C. Yui, Gary M. Swift, Carl Carmichael, Rocky Koga and Jeffrey S. George, Poster Session).

5) *Los Alamos National Laboratories (LANL)*

Group NIS-3, Space Data Systems, Mail Stop D440
Nonproliferation and International Security Division
Los Alamos National Laboratory, Los Alamos, NM 87545
Phone: (505) 667-7024

- Michael Caffrey: mpc@lanl.gov

- Paul Graham: grahamp@lanl.gov

Contribution:

- Fault injection for the Virtex-I and Virtex-II

6) *MD Robotics*

9445 Airport Road
Brampton, Ontario, Canada L6S 4J3
Phone: 905-790-2800 Fax: 905-790-4400

- David Hiemstra: dhiemstra@mdrobotics.ca

Contribution:

- Participation in the radiation testing experiments
- Data acquisition and analysis
- Provided beam time in the TRIUMPH facility (Vancouver, Canada)

7) *Sandia National Laboratories*

Albuquerque, NM, USA

- Kurt Lanes: krlanes@sandia.gov
- Mathew Napier: mpnapie@sandia.gov
- Ted Wrobel: tfwrobe@sandia.gov

Contribution:

- Co-funding of the TMR tool
- Co-funding for the use of heavy ion facilities (dynamic testing)
- Static testing data review and analysis
- Development of the test methodology for the IO and the clock structures (DCM)
- Analysis of TMR IO signal integrity

8) *SEAKR Engineering, Incorporated*

Aerospace Data Storage and Processing Solutions
6221 So. Racine Circle, Centennial, Colorado 80111
Phone: (303) 790-8499

- Tilan Langley: tilan.langle@jpl.nasa.gov
- Paul Murray: paul@seakr.com

Contribution:

- Design and fabrication of the 2V6K Dynamic Test Board
- Assistance with the data acquisition

9) *UB Computer*

Phone: (630) 235-3530

- Geoff Woodcock: geoff@ubcomputer.com

Contribution:

- Development of FIVIT software tool for radiation test experiments
- Development of the TMR tool

10) *USC Information Sciences Institute (ISI)*

USC Information Sciences Institute (ISI)

3811 North Fairfax Drive, Suite 200

Arlington, VA 22203

Phone: (703) 812-3722

- Peter Bellows: pbellows@isi.edu
- Brian Schott: bschott@east.isi.edu

Contribution:

- Providing web archive for consortium email

11) *Xilinx Inc.*

2100 Logic Drive

San Jose, CA 95124-3400

Phone: (408) 559-7778

- Brendan Bridgford: brendanb@xilinx.com
- Carl Carmichael: carlc@xilinx.com
- Joe Fabula: joef@xilinx.com
- Jason Moore: jasonm@xilinx.com
- Sana Rezgui: sanar@xilinx.com

Contribution:

- Development of the FIVIT software tool for radiation test experiments
- Fault injection for the Virtex-I and Virtex-II
- Development of the TMR tool

- Design of the JPL/XILINX 2V1K dynamic test board
- Test (static and 2V1K dynamic) vehicle design and preparation
- Design of the SEAKR 2V6K Dynamic test Board
- Data acquisition and analysis
- Test methodology for the 2V6K dynamic testing
- Provided beam time at Texas A&M, UC Davis, and Indiana and Berkeley facilities (heavy ions, protons)
- Provided the Virtex FPGA (3K and 6K) and the PROM circuits
- Development of the Consortium Website
- Publication of the test results at NSREC and RADECS 2003

II. VIRTEX-II OVERVIEW

The Xilinx Virtex-II device is an SRAM-based in-system configuration, most suited for use in many telecommunication, wireless, networking, video, and DSP applications, including those in space. The main functional elements in a Virtex II are comprised of Input/Output Blocks (IOBs) and internal functional blocks.

The internal functional blocks include 4 major elements:

- Configurable Logic Blocks (CLB), which provides functional elements for combinatorial and synchronous logic, including basic storage elements BUFTs associated with each CLB drive
- Block SelectRAM memory modules provide large 18 K-bit storage elements of true dual Port RAM
- Multiplier blocks are 18 bit x 18 bit dedicated multipliers
- DCM (Digital Clock Manager) blocks

The IOBs include mainly:

- Input Block with an optional single data rate or double data rate DDR register
- Output Block with an optional 3-state single data rate or register and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bi-directional block

The IOBs support the following single-ended I/O standards:

- LVTTTL, LVCMOS
- PCI-X at 133MHz, PCI (3.3V at 33MHz and 66MHz)
- GTL and GTLP
- HSTL (Class I, II, III and IV)
- SSTL
- AGP-2X

The digitally controlled Impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element. Table 1 summarizes the features of the Virtex-II (2V1000, 2V3000, and 2V6000). Detailed information about the Virtex-II family devices is provided in the Virtex-II Platform FPGA Handbook.

Table 1: Cursory description of Virtex-II parts used in radiation tests

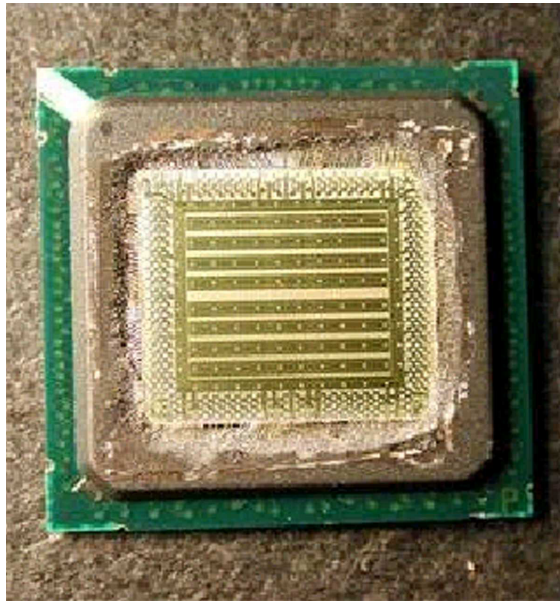
Virtex-II Device	2V1000	2V3000	2V6000
Configuration Bits	2,787,740	7,347,524	16,395,508
Block SelectRAM Bits	737,280	1,769,472	2,654,208
IOBs (Maximum)	432	720	1,104
Multiplier Blocks	40	96	144
DCMs	8	12	12

III. DEVICES UNDER TEST

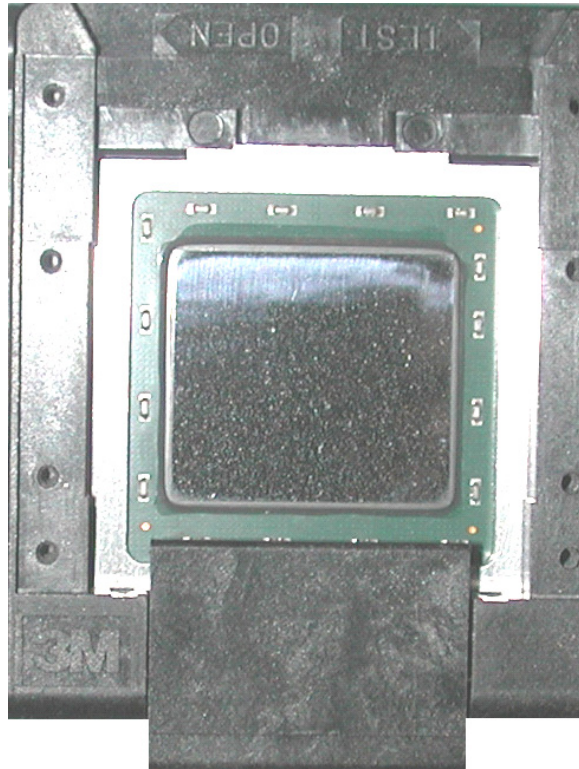
All test devices have a 1.5 V core and are manufactured on 0.15 μ m/0.12 μ m CMOS, 8-layer metal process with a thin epitaxial layer for latch-up resistance. The 2V1000-FG256 and the 2V3000-FG676 were ideal for SEU characterization, as they have a face-up die configuration, suitable for heavy ion penetration. Prior to testing, each device was chemically etched to expose the die. Evaluation samples of the 2V1000 were packaged in a commercial 256-pin wire-bond fine pitch ball grid array (FG) package. The packages were de-capped with chemical etching to expose the die to heavy ions. The 2V1000 part includes 40 block RAMs of 18 Kbits, 172 I/Os, and 2,787,740 configuration bits. The 2V3000 samples were packaged in 676-pin wire-bond fine pitch ball grid array (FG) package. It includes 96 block RAMs of 18 Kbits, 720 I/Os, and 7,347,524 configuration bits.

However, the 2V6000-FF1152 is only available as a flip-chip mounted device requiring backside die thinning from \sim 800 μ m to \sim 200 μ m and irradiation through the remaining substrate material. Although this was not a problem for static characterization, the 2V6000 could not be utilized for latch-up testing. The 2V6000 was packaged in a commercial 1152-pin flip-chip fine-pitch device (FF) package. It comprises 144 block RAMs of 18 Kbits, 824 I/Os, and 16,395,508 configuration bits.

Figure 1 depicts photos of a 2V1000 (Figure 1 a) and a 2V6000 (Figure 1 b) used for testing. Epitaxially grown samples parts were used for latch-up verification. Most of the lower LET static testing was performed on non-epitaxial samples of identical mask set design.



a) Etched 2V1000



b) Thinned 2V6000

Figure 1: Examples of Delidded Test Devices

IV. EXPERIMENTAL SET-UP

The main objective of this test was to capture the post-irradiation configuration and block SelectRAM data through the SelectMAP and JTAG configuration interfaces of the DUT. Single-event-upsets (SEU) and single-event functional interrupts (SEFI), which might occur while exposing the device to heavy ions or protons beams, are counted and recorded. For these purposes, a test platform was built, which comprises a *HW-AFXBG256-200* prototype board connected to a host PC running custom test software (named FIVIT “Fault Injection and Verification Tool”) via Xilinx’ MultiLinx cable and the Xilinx Parallel III, JTAG cable (Fig. 2). This software, a specifically designed C⁺⁺ based application, is used to check communication between the DUT and the interface cables as well as to determine the number of upsets in the configuration memory, block SelectRAM memory cells, user flip-flops and control registers after each subsequent configuration and beam run.

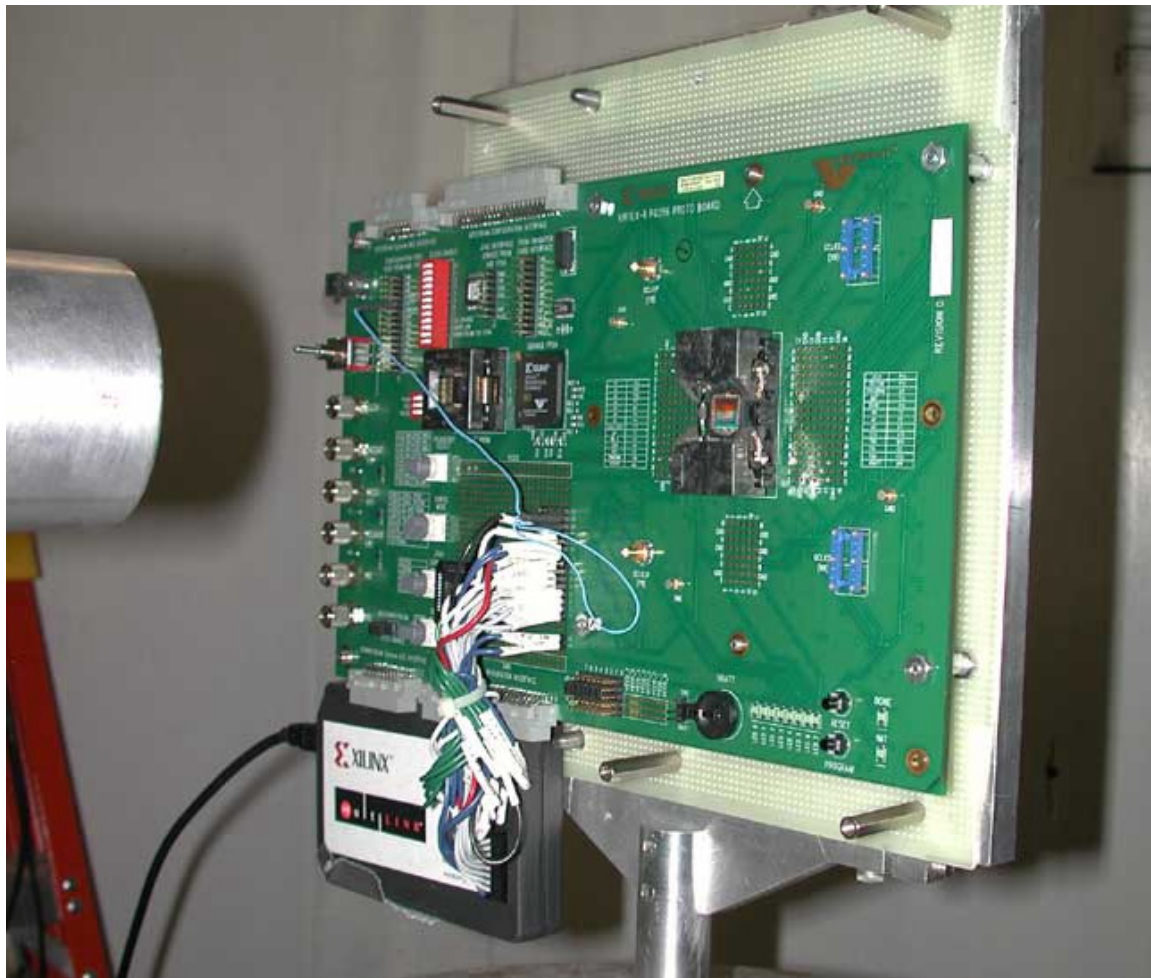


Figure 2: HW-AFXBG256-200 prototype board connected to the host PC and test software via Xilinx’ MultiLinx cable in front of beam at Texas A&M

The FiViT application is used to load and readback the configuration data of an FPGA. Some additional features of FIVIT include the ability to set all user flip-flops to either '1s' or '0s', capture their data, and read and write to configuration control registers (through either the MultiLinx slave SelectMAP mode or through the JTAG cable). The control registers examined during testing are the command register (CMD), frame length register (FLR), configuration option register (COR), masking register for CTL (MASK), control register (CTL), frame address reader (FAR), CRC register and the status register (STAT). This utility was incorporated in later test runs after previous heavy ion tests revealed functional interrupts that disabled the SelectMAP port. Some of these interrupts were the result of upsets in these registers, which could have been corrected prior to data acquisition. Figure 3 is a screen capture of this program.

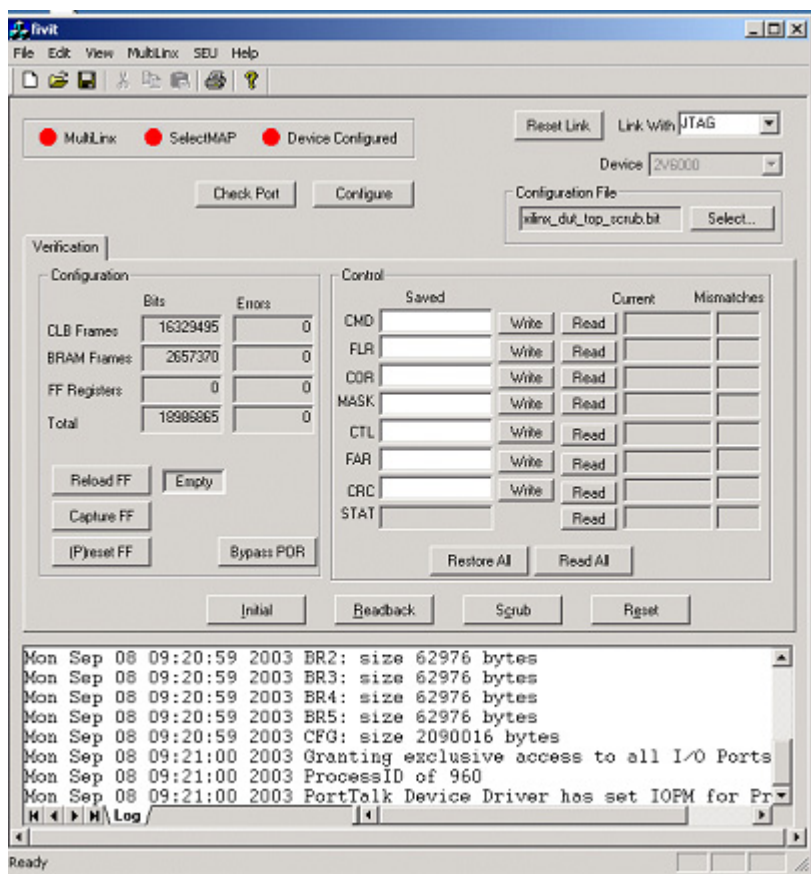


FIGURE 3: SCREEN CAPTURE OF THE FIVIT SOFTWARE

An HP6629A digital power supply was used to provide 3.3 V to the board and FPGA IO. 1.5V was supplied to the FPGA core. A separate laptop was connected to the HP6629A to strip chart the two voltage and current readings.

IV. LATCHUP TESTING

Virtex-II latch-up testing was performed at the Texas A&M cyclotron in June and November of 2003. The XQR2V3000-FG676 device used in these latchup tests was manufactured on a thin epitaxial substrate. To date, no additional devices of the Virtex II family of FPGAs was tested for latchup. All experiments were conducted using 15MeV/amu gold ions. The stopping power of the ions was changed by altering the angle of incidence between normal incidence and 60 degrees. Table 2 summarizes the change in range and stopping power as a function of incident angle. The applied fluxes were typically of an order of magnitude of 10^5 particles/cm²/s and multiple runs were conducted in order to obtain the total fluences shown in Table 2.

Table 2: Main Characteristics of Used Heavy Ions Beams

Heavy Ion	Angle	Degrader	Effective LET [MeV/mg/cm ²]	Energy [MeV/u]	Range [μm]	Fluence [particles/cm ²]
Au	60	none	163	15	72	1×10^7
Au	30	none	103.8	15	71	4×10^7
Au	0	none	80.2	15	155	2×10^7

For the purpose of this experiment, the accepted definition of a latch-up condition was any error mode resulting from the test run that required a power cycle of the DUT in order to recover. During the test runs, the DUT core and IO voltages and current consumption were captured and recorded in a running log (strip chart). Maximum current triggers were set on the power supplies in the event of a latch-up condition that would result in excessive current draw. Due to the high fluxes and total fluences used for the latch-up testing, it was expected that the DUT would lose its programming early in the run and would likely be subject to multiple SEFI conditions during the run. The purpose of the experiment is to demonstrate hardware survivability and soft recovery without the need for a device power cycle. Therefore, the test procedure adopted is as follows:

- Program and readback verify DUT
- Irradiate DUT
- Record DUT conditions and any anomalous observations or behavior
- Program and readback verify DUT

The Virtex-II XQR2V3000 devices showed no latchup during our Au heavy ion irradiation test up to an LET of 160 MeV-cm²/mg and total fluences of 7×10^7 particles/cm².

V. STATIC TESTING

The static SEU experimentation was performed on the following devices: the 2V1000, the 2V3000, and the 2V6000. The purpose of these experiments was to determine the saturation cross section and threshold of upsets in the configuration and block SelectRAM memory cells. In addition, the experimental methods were devised in such a way to maximize the visibility of any SEFI conditions. Occasionally, the experimental method and/or equipment would be revised to enhance visibility as new error modes were discovered. Some details about this work were previously presented at the MAPLD international conference, 2002 [1]. Throughout the document, test results from the Texas A&M (TAM) and the Lawrence Berkeley Laboratory (LBL) facilities are reported separately. The data from either test facility agree on the saturation cross section, but show a marked difference in the cross section threshold. Furthermore, the consortium members noted a Weibull and Edmonds parametric fit to the LBL data that is uncharacteristically steep at the LET threshold. At this point the differences in the cross section threshold are not understood and an unresolved systematic error is the suspected cause for the discrepancy. A more detailed discussion of possible systematic errors is presented in the “Configuration Memory Cell and Block Ram Cell” section below.

A. DUT Test Configuration Designs

Several FPGA design configurations were used to program the 2V1000, 2V3000, and 2V6000 devices prior to irradiation. The “2v1000_ff_capture” design implemented in the FPGA is a shift register design that may be re-initialized to all ‘1’s or all ‘0’s. The capacity of the shift register used is (320x32) 10240 flip-flops. The “2v1000_ff_checker” design implemented a similar shift register design that would initialize to a “checker-board” (alternating ones and zeros) pattern. The “2v1000_ff_default”, “2v3000_ff_default” and “2v6000_ff_default” designs were functionally void designs that configured only the CAPTURE_VIRTEX2 architectural element. The CAPTURE element is a programmable user resource that is used to load CLB flip-flop values into shadow cell locations within the configuration memory so that the values may be captured upon configuration readback. The same operation was also executed without the use of the Capture element by the use of CMD register commands. The results issued from heavy ions and proton radiation testing is described below.

B. Heavy Ions Testing Results

Heavy ions testing experiments were performed at the Cyclotron Institute, Texas A&M University in June, August, and November 2002 and at Berkeley National Laboratory, UC Berkeley in October 2002. Heavy ions cocktails were Xenon (Xe), Krypton (Kr), Copper (Cu), Argon (Ar) Neon (Ne), Nitrogen (N), and Boron (B). Main characteristics of the heavy ion beams to which the Virtex-II were exposed as well as the selected device (2V1000, 2V3000, and 2V6000) sensitivities to those beams are given in Table 3.

Table 3: Measured Heavy Ion Cross Sections

a) for the 2V6000 testing at TAM facility

Heavy Ion	Effective LET [MeV/mg/cm ²]	Energy [MeV/u]	Range [μm]	Fluence [particles/cm ²]	Cross Section CLBs [cm ²]	Cross Section BRAM [cm ²]
Xe	63.3	24.8	27	1.00x10 ⁶	1.21E-08	1.54E-08
Xe	61.3	24.8	51	0.50x10 ⁶	1.77E-08	2.43E-08
Xe	55.5	24.8	88	0.50x10 ⁶	2.59E-08	3.69E-08
Xe	53.0	24.8	108	0.98x10 ⁶	3.59E-08	4.52E-08

b) for the 2V3000 testing at TAM facility

Heavy Ion	Effective LET [MeV/mg/cm ²]	Energy [MeV/u]	Range [μm]	Fluence [particles/cm ²]	Cross Section CLBs [cm ²]	Cross Section BRAM [cm ²]
Au	142	24.8	146	5.80x10 ³	4.65E-08	8.70E-08
Au	115	15.0	147	5.00x10 ³	3.96E-08	3.96E-08
Xe	88	24.8	(96, 32)*	4.50x10 ⁴	3.79E-08	5.31E-08
Xe	80.9	15.0	150	2.00x10 ⁴	4.96E-08	6.21E-08
Au	76.1	24.8	(113, 72)*	4.00x10 ⁴	3.47E-08	5.00E-08
Xe	61.2	24.8	(143, 52)*	3.00x10 ⁴	3.32E-08	4.03E-08
Kr	44.3	24.8	(120, 66)*	2.00x10 ⁴	2.50E-08	3.36E-08
Xe	42.8	24.8	208	2.00x10 ⁴	3.06E-08	3.18E-08
Kr	38.4	24.8	(140, 42)*	2.00x10 ⁴	2.46E-08	2.75E-08
Kr	30.8	24.8	(176, 98)*	2.00x10 ⁴	2.40E-08	2.75E-08
Kr	21.6	24.8	254	2.00x10 ⁴	2.10E-08	2.48E-08
Ar	18.5	15.0	(75, 43)*	2.00x10 ⁴	1.36E-08	1.84E-08
Ar	16.0	15.0	(89, 63, 32)*	2.00x10 ⁴	1.37E-08	1.84E-08
Ar	12.8	15.0	(113, 65)*	2.00x10 ⁴	1.24E-08	1.70E-08
Ar	8.89	15.0	165	2.00x10 ⁴	9.15E-09	9.15E-09
Ar	7.94	40.0	493	1.00x10 ⁵	9.88E-09	9.88E-09
Ar	6.91	40.0	568	1.01x10 ⁵	6.85E-09	1.04E-08
Ne	5.80	15.0	119	2.00x10 ⁴	6.66E-09	1.04E-08
Ar	5.59	40.0	703	9.99x10 ⁴	6.25E-09	6.25E-09
Ne	5.02	15.0	139	2.00x10 ⁴	6.10E-09	8.62E-09
Ne	4.04	15.0	174	2.02x10 ⁴	6.00E-09	6.00E-09
Ar	3.94	40.0	1001	8.99x10 ⁴	5.44E-09	7.71E-09
Ne	3.00	15.0	260	1.97x10 ⁴	5.15E-09	5.15E-09
Ne	2.45	40.0	774	2.00x10 ⁵	2.79E-10	2.79E-10
Ne	2.13	40.0	775	4.00x10 ⁵	2.49E-10	1.20E-10
Ne	1.72	40.0	776	3.00x10 ⁵	1.66E-10	1.51E-10
Ne	1.22	40.0	778	2.5x10 ⁵	1.13E-10	8.59E-11

c) for the 2V1000 testing at LBL facility

Heavy Ion	Effective LET [MeV/mg/cm ²]	Energy [MeV/u]	Range [μm]	Fluence [particles/cm ²]	Cross Section CLBs [cm ²]	Cross Section BRAM [cm ²]
Xe	63.3	4.50	35	3.49x10 ⁶	4.00E-08	3.69E-08
Kr	40.6	4.50	29	7.96x10 ⁵	3.00E-08	3.52E-08
Cu	32.0	4.50	27	4.07x10 ⁶	1.78E-08	2.20E-08
Ar	16.2	4.50	30	1.44x10 ⁶	2.74E-08	3.58E-08
Ne	6.62	4.50	37	2.45x10 ⁶	2.12E-08	3.07E-08
N	2.99	4.50	61	1.73x10 ⁶	1.87E-08	2.51E-08
B	1.82	4.50	63	2.63x10 ⁷	2.18E-09	1.01E-10

d) for the 2V1000 testing at TAM facility

Heavy Ion	Effective LET [MeV/mg/cm ²]	Energy [MeV/u]	Range [μm]	Fluence [particles/cm ²]	Cross Section CLBs [cm ²]	Cross Section BRAM [cm ²]
Xe	61.3	24.8	51	2.25x10 ⁶	3.70E-08	4.19E-08
Xe	57.2	24.8	77	5.01x10 ⁴	3.26E-08	3.86E-08
Xe	52.9	24.8	(109, 174)*	2.90x10 ⁶	4.37E-08	3.96E-08
Xe	48.8	24.8	143	2.25x10 ⁶	3.20E-08	4.11E-08
Xe	46.4	24.8	166	4.07x10 ⁶	2.91E-08	3.31E-08
Xe	44.0	24.8	193	2.00x10 ⁵	2.91E-08	3.59E-08
Xe	41.7	24.8	223	1.03x10 ⁷	3.07E-08	3.43E-08
Kr	34.9	40.0	59	2.02x10 ⁵	2.18E-08	2.82E-08
Kr	28.5	40.0	117	1.98x10 ⁵	1.99E-08	2.44E-08
Kr	21.0	25.0	273	5.42x10 ⁶	1.87E-08	2.40E-08
Kr	14.9	40.0	559	3.99x10 ⁵	1.46E-08	1.97E-08
Ar	12.2	40.0	73	6.42x10 ⁶	1.18E-08	1.57E-08
Ar	9.84	40.0	128	4.02x10 ⁶	9.43E-09	1.38E-08
Ar	8.95	40.0	163	1.20x10 ⁷	9.10E-09	1.32E-08
Ar	7.89	40.0	217	9.00x10 ⁶	8.26E-09	1.23E-08
Ne	5.76	25.0	457	2.84x10 ⁷	7.71E-09	1.02E-08
Ar	3.92	40.0	1016	3.00x10 ⁶	6.19E-09	8.88E-09
Ne	2.15	40.0	455	1.57x10 ⁷	2.16E-09	1.13E-09
Ne	1.80	24.8	735	4.05x10 ⁸	2.85E-09	6.79E-10
Ne	1.21	40.0	1593	3.55x10 ⁷	1.30E-10	8.46E-11

*Multiple range and/or LET values obtained with degraders.

Devices were tested at different incidences for an LET range of 1.2 – 63.3 MeV-cm²/mg. The average fluence was 10⁵ particles/cm². Each experiment was repeated several times (at least 5 runs for each used heavy ions beam). A vacuum chamber was used at the Lawrence Berkeley test facility. The saturation cross sections measured at both the Texas A&M and LBL cyclotrons were consistent. However, some discrepancies between the results obtained at the two facilities have been noted for the cross sections at lower LETs. Two models have been considered to fit the obtained data in curves:

- a physically based (diffusion) model of Larry Edmonds with two parameters:

$$\sigma(LET) = \sigma_{sat} \exp(-[(L_{1/e}) / LET]) \quad (1)$$

σ_{sat} (a fitting parameter) is the saturation cross section,
 $L_{1/e}$ (another fitting parameter) is the LET at which the cross section is reduced to 1/e times (or ~36.79% of) the saturation cross section.

- a Weibull model with four fitting parameters:

$$\sigma(LET) = \sigma_{sat} (1 - \exp\{ -[(LET - L_{th}) / W]^S \}) \quad (2)$$

σ_{sat} is the limiting or plateau cross section (or “limit”),

L_{th} is the LET threshold parameter (or so called “onset”),

W is the width parameter, and

S is a dimensionless exponent dubbed “power.”

The next subsection presents the measured static sensitivities of the configuration memory cells and also the block RAM cells sensitivities to upsets while the subsection after that presents SEFI results classified into two categories: POR-like and communication loss.

1) Configuration Memory Cells and Block RAM Cells

Table 4 shows the selected parameters for the drawing of the Edmonds and Weibull curves ($L_{1/e}$, σ_{sat} , onset, power, width, limit). The device’s sensitivities to upsets are given in Figures 4, 5, 6, and 7. Figures 4 and 5 show the device’s responses to heavy ions beams at Texas A&M cyclotron, while the graphs given in Figures 6 and 7 correspond to obtained data in the LBL facility. Note that the fits have been adjusted upwards slightly to enclose as many data points as possible. In addition, the graphs include only data points issued from tested devices at normal incidence. Indeed, the analysis of the obtained results proved that the data points taken at an incidence different from 0, are always lower than the rest of the data set. This led to the exclusion of those points from the graphs that represent the configuration and BRAM bits responses to heavy ion beams. However, they have been included in the SEFIs’ graphs in order to get more statistics. The configuration bits and BRAM cross sections corresponding to the complete data set, at normal incidences as well as at other incidences, are displayed in Figures 16 and 17 in Appendix I.

Table 4: Edmonds and Weibull Parameters for Configuration Cells Sensitivities to SEUs

Parameters	Edmonds		Weibull			
Cells	$L_{1/e}$	σ_{sat} MeV-cm²/mg	Limit Cm²	Onset MeV-cm²/mg	Width -	Power -
Configuration bits – TAM (Fig 4)	5.3	3.8E-8	4.37E-8	1.0	33	0.8
Configuration bits – LBL (Fig 5)	2.0	3.5E-8	4.00E-8	1.5	7	0.3
BRAM - TAM (Fig 6)	7.0	4.7E-8	4.19E-8	1.0	17	0.9
BRAM - LBL (Fig 7)	1.7	4.0E-8	3.69E-8	1.2	2	0.8

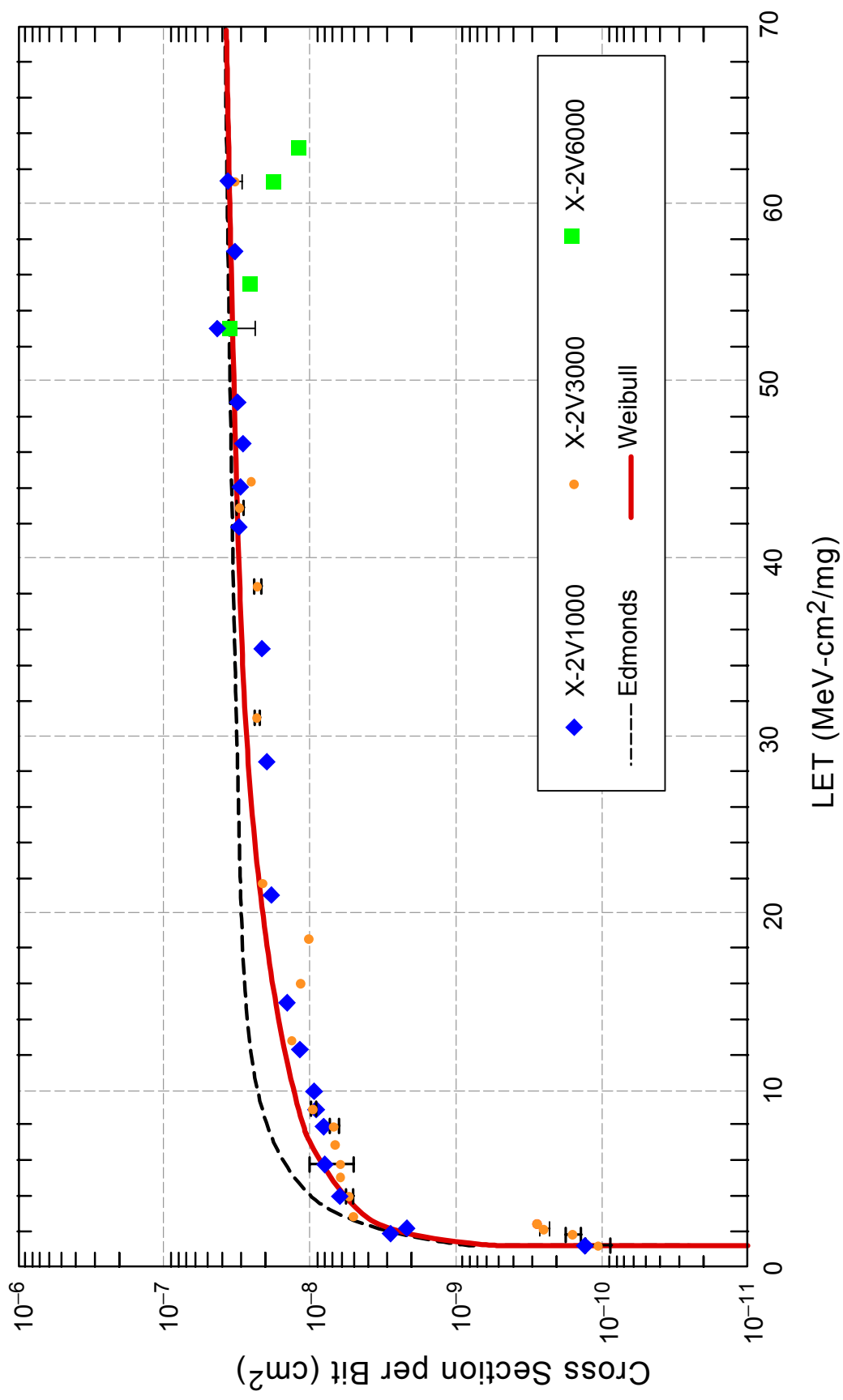


Figure 4. Virtex-II Configuration Memory Cells (Texas A&M)
Heavy Ion SEU Cross Sections for the X-2V1000, X-2V3000, and X-2V6000

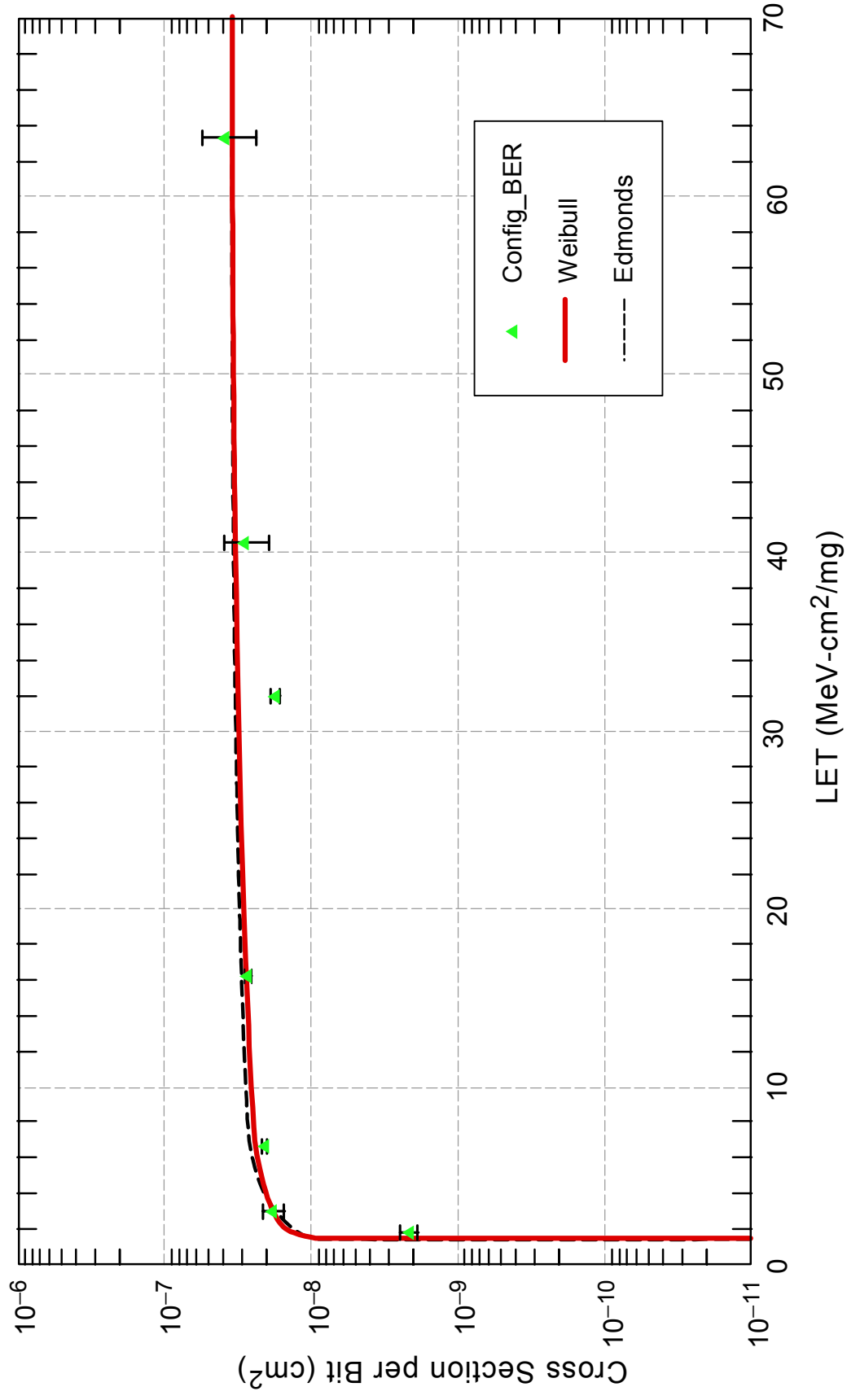


Figure 5. Virtex-II Configuration Memory Cells (LBL)
Heavy Ion SEU Cross Sections for the X-2V1000

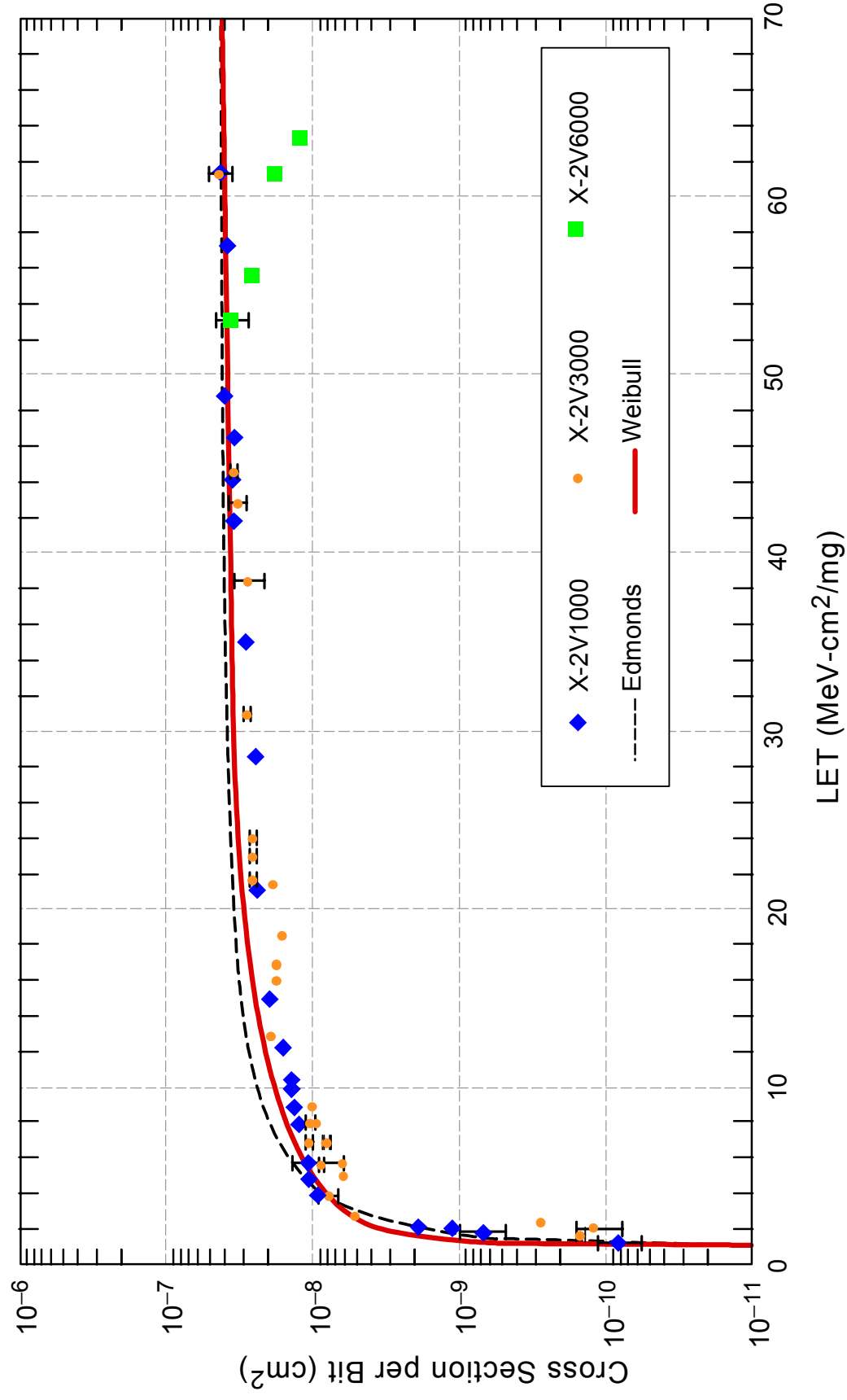


Figure 6. Virtex-II Block Memory Cells (Texas A&M)
Heavy Ion SEU Cross Sections for the X-2V1000, X-2V3000, and X-2V6000

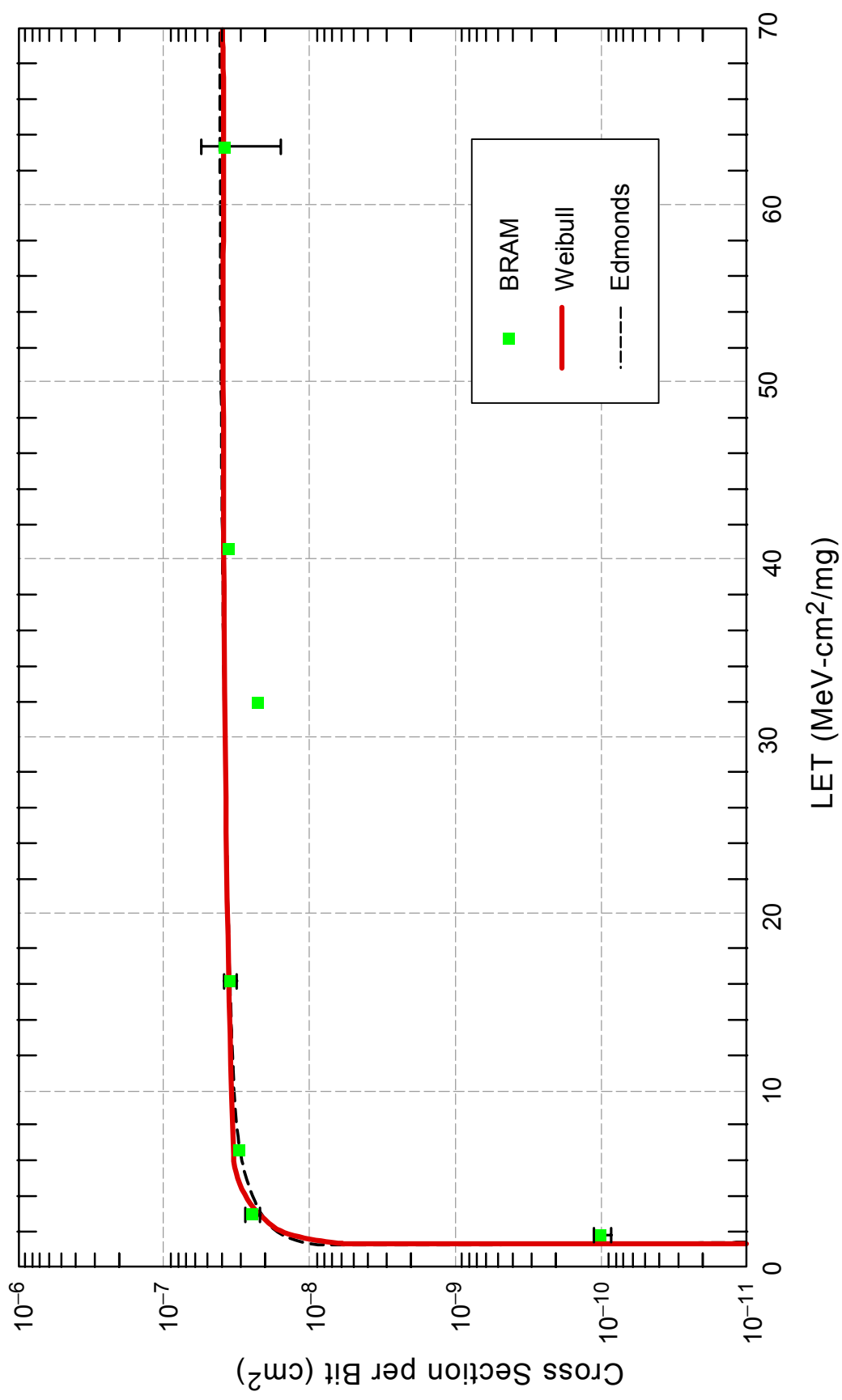


Figure 7. Virtex-II Block Memory Cells (LBL)
Heavy Ion SEU Cross Sections for the X-2V1000

As shown in Figures 4, 5, 6 and 7, the device exhibited upsets starting at an LET of about 1 MeV-cm²/mg, for both the configuration memory and the block memory cells. The saturation cross sections of the configuration memory and block memory cells, were found to be approximately 4.E-8 cm²/bit, both at LBL as well as at Texas A&M. However, the results obtained at the two facilities differ by as much as an order of magnitude for lower LETs (less than 20 MeV-cm²/mg) for both configuration and block RAM cells.

The following possible explanations have been offered by various consortium members to explain these differences in the results from either laboratory:

- Differences in the beam characteristics, e.g., the shorter range of the LBL beams
- Incorrect dosimetry of particle fluence at one (or both) facilities (Note that the data from several Texas test dates is self-consistent, but with only one LBL date, a consistency check is not possible.)
- Beam contamination from another ion species (Note that LBL uses a “cocktail” in their ion sources to allow rapid beam changes.)

Further investigations are needed to explain this discrepancy between the LBL and the Texas A&M data and these investigations have not yet been undertaken.

In addition, the results issued at Texas A&M facility show that the 2V1000 and the 2V3000 are having the same sensitivity per bit to heavy ion beams, while the 2V6000 is slightly less sensitive per bit than the 2V1000 or the 2V3000. This difference (between the 2V6000 and the 2V1000 or the 2V3000) was unexpected since the memory cell layouts are identical. More radiation testing is needed to determine precisely the 2V6000 sensitivities to SEUs. This will be accomplished as part of the next major consortium objective: Dynamic Functional and Mitigation testing, which will focus primarily on the 2V6000.

In addition to the upset susceptibility of the configuration and BRAM bits, the DUT is susceptible to single-event-functional-interrupts (SEFIs) which are caused by SEU(s) within control logic elements. The device’s sensitivities to such events have been measured, and those results are presented in the next sub-section.

2) Single Event Functional Interrupt (SEFI)

Typically, SEFIs are low in occurrence and are almost never seen while in orbit. However, in test environments where event rates are hugely accelerated in order to mimic conditions of a worse-case example of the intended use of the test device, SEFIs can be observed. The criterion for a SEFI for the Virtex-II is that it requires a complete reconfiguration of the device before returning to normal operability, but does not require a power cycle. Three single-event-functional-interrupt (SEFI) categories have been observed. They include the power-on-reset (POR) SEFI, SelectMAP SEFI, and a JTAG Configuration Access Port (JCFG) SEFI and are results of ion hits to the corresponding circuitry.

The POR SEFI results in a global reset of all internal storage cells and the loss of all program and state data. Observation of this mode was noted by a sudden decrease of the DUT current to its starting value. As configuration upsets within the device were generated during the beam run, the DUT current increased as errors were allowed to accumulate. A sudden extreme decrease of the DUT current to its starting value would indicate a POR SEFI. Once this mode has occurred, no other data could be taken and thus the run would be terminated as quickly as possible in order to record an accurate fluence measurement.

At the end of a run, a SelectMAP SEFI would be indicated by the retrieval of only meaningless data from SelectMAP Port. In a few cases, the port could be re-activated by using the JTAG port to find and correct errors in the control registers. In the remaining occurrences, a complete reconfiguration was required to regain SelectMAP access.

The JCFG SEFI deactivates configuration memory read/write access from JTAG Port and is detected by a constant value being returned by the configuration memory read operation. In some cases, the JTAG port could still successfully access all control registers but not the configuration memory array. The system impact of both the SelectMAP and JCFG SEFI would be the inability to scrub (correct) individual upsets in the configuration memory requiring a reconfiguration of the FPGA and a disruption to service. However, prior to reconfiguration and in the absence of other upsets within the configuration memory array, the user's design would still be fully functional even after the loss of configuration communications.

The selected parameters to draw the Weibull and Edmonds curves are given in Table 5, and the cross section curves for the major SEFI modes are displayed in the following graphs (Figures 8 – 10).

Table 5: Edmonds and Weibull Parameters for SEFIs curves under heavy ion beams

Parameters	Edmonds		Weibull			
	$L_{1/e}$	σ_{sat} MeV-cm ² /mg (MeV)	LIMIT Cm ²	ONSET MeV-cm ² /mg (MeV)	WIDTH -	POWER -
POR	-10.3	3.0E-6	2.50E-6	1.5	22	1.2
SMAP	-7.5	1.9E-6	1.72E-6	1.5	17	1.0
JCFG	-8	3.4E-7	2.51E-7	1.5	17	1.0

Table 6: Measured Heavy Ion SEFI Cross Sections

Heavy Ion	Effective LET [MeV/mg/cm ²]	Energy [MeV/u]	Range [μm]	Fluence [particles/cm ²]	POR SEFI Cross Section [cm ²]	SMAP SEFI Cross Section [cm ²]	JCFG SEFI Cross Section [cm ²]
Xe	63.3	24.8	35	4.51E+06	1.11E-06	4.43E-07	2.22E-07
Xe	61.3	24.8	51	2.45E+06	8.89E-07	4.08E-07	1.00E-55
Kr, Xe	52.9	24.8	(109, 174)*	2.99E+06	3.04E-06	1.34E-06	1.00E-55
Kr	50	24.8	143	1.16E+06	1.72E-06	1.72E-06	1.00E-55
Xe	46.4	24.8	166	4.07E+06	2.21E-06	1.47E-06	1.00E-55
Kr	41	24.8	223	1.13E+07	9.70E-07	1.15E-06	9.49E-08
Kr, Cu	29.9	40.0	117	3.98E+06	1.26E-06	7.54E-07	2.51E-07
Kr	21.0	25.0	273	5.42E+06	1.29E-06	1.11E-06	1.00E-55
Ar	16.2	4.50	30	3.97E+06	2.52E-07	1.76E-06	1.00E-55
Ar	12.2	40.0	73	6.42E+06	4.67E-07	4.67E-07	1.00E-55
Ar	11.7	25.00	211	1.11E+07	5.41E-07	3.60E-07	1.00E-55
Ar	9.84	40.0	128	4.02E+06	1.00E-55	2.49E-07	1.00E-55
Ar	8.95	40.0	163	1.20E+07	1.67E-07	5.00E-07	1.00E-55
Ar	7.89	40.0	217	9.00E+06	2.22E-07	1.11E-07	1.00E-55
Ar, Ne	7	24.8	85	7.26E+06	2.76E-07	1.38E-07	1.00E-55
Ne	6.62	4.50	37	2.45E+06	4.09E-07	4.09E-07	1.00E-55
Ne	5.76	25.0	457	2.84x10 ⁷	2.82E-07	1.41E-07	1.00E-55
Ar	5.55	40.00	714	1.99E+06	1.00E-55	1.00E-55	1.00E-55
Ne	4.31	40.00	228	1.20E+07	1.00E-55	8.33E-08	1.00E-55
Ne	3.7	40.0	1016	2.31E+07	1.00E-55	8.65E-08	1.00E-55
Ne	3	40.00	396	1.68E+07	1.19E-07	1.78E-07	1.00E-55
Ne	2.4	40.00	520	8.12E+07	1.23E-08	3.70E-08	1.00E-55
Ne	2.15	40.0	455	1.70E+07	1.00E-55	1.00E-55	1.00E-55
Ne, B	1.80	24.8	(1122, 735, 63)*	2.99E+08	1.00E-08	1.00E-08	1.00E-55
Ne	1.21	40.0	1593	3.55E+07	1.00E-55	1.00E-55	1.00E-55

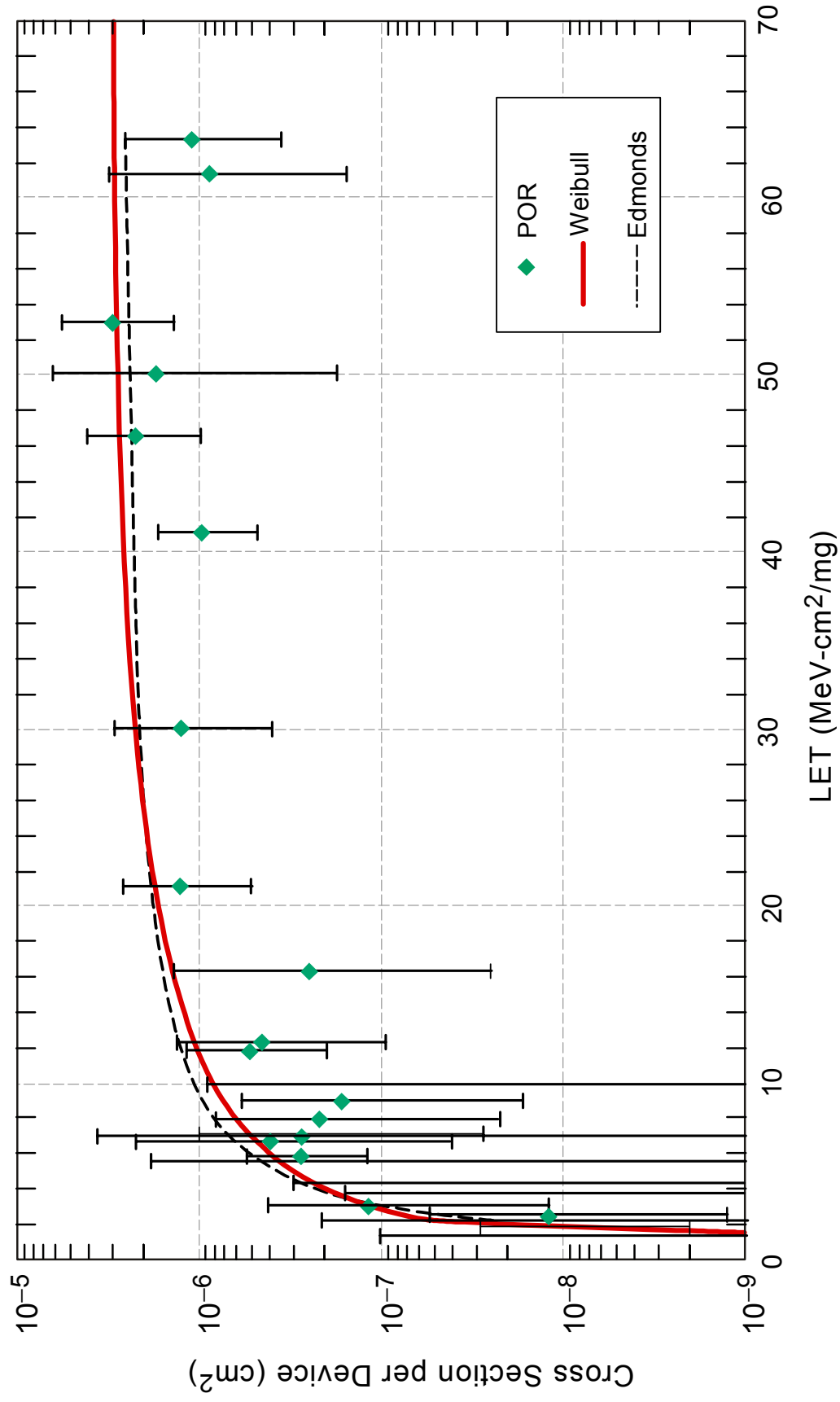


Figure 8. Virtex-II POR SEFI Cross Section

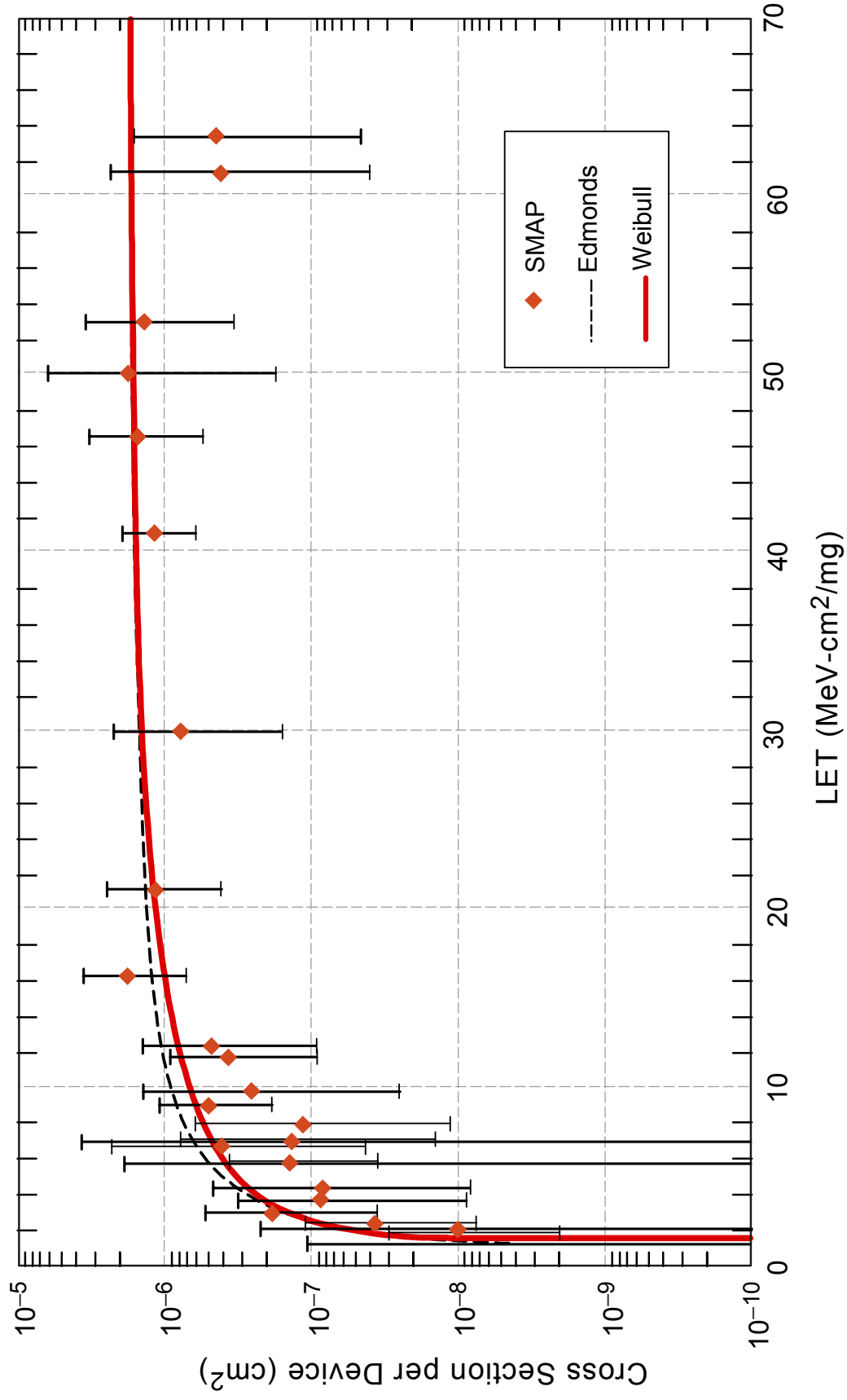


Figure 9. Virtex-II SMAP SEFI Cross Section

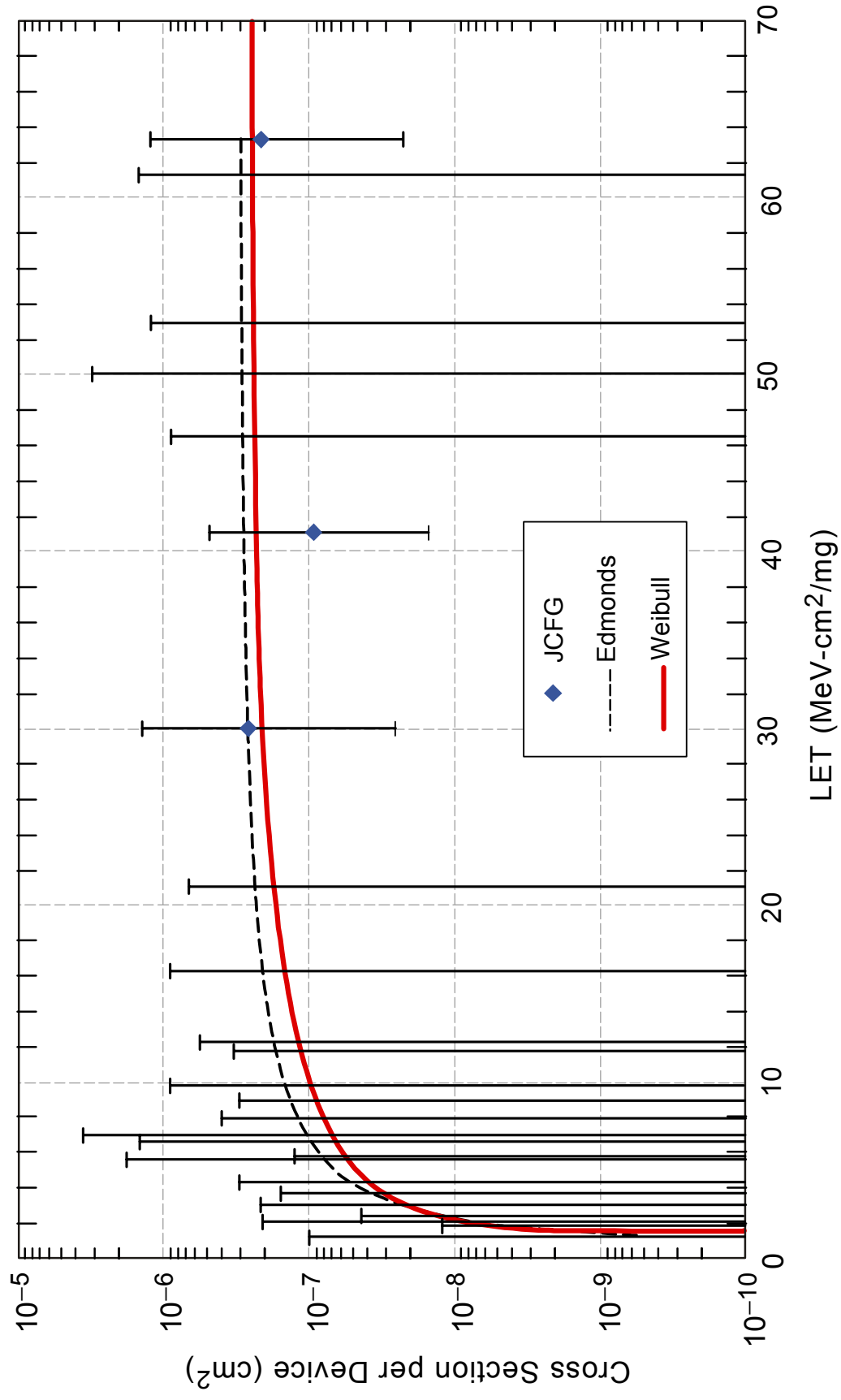


Figure 10. Virtex-II JCFG SEFI Cross Section

Heavy ions altering the logic states of the POR circuitry and SelectMAP port were two of the more frequently occurring SEFIs, either disabling the communication between the FIVIT software or resetting the device. A few other SEFI types were identified, including events affecting the ability to read and/or write configuration registers. These were quite rare and would require even more testing to measure the individual cross sections so they have been lumped in with the POR-type SEFI “basket.” Other types of errors that occurred but do not lead to functional interrupts comprise of bit flips to configuration registers such as the frame length register (FLR), configuration option register (COR), and frame address reader (FAR). These errors were correctable and, after doing so, valid configuration data was read.

3) Protons Testing Results

Proton radiation testing were performed at IUCF in February 2002, at LBL in January 2003 and at the Crocker Nuclear Laboratory, UC Davis (UCD) in February, April, May and June 2002. Tables 7 and 9 summarize the main features of the used protons’ beams as well as the device’s sensitivities to SEUs and SEFIs. The beams’ characteristics that have been used for the 2V6000 testing are highlighted in gray. As shown in Table 5, the applied fluxes were, in most cases, higher than 10^9 , while the fluences vary between 10^{11} and 10^{13} particles/cm².

Table 7: Measured Cross Sections under Protons’ Beams

Energy [MeV]	Facility	Exposed Part Virtex-II-	Fluence [particles/cm ²]	CLB Section [cm ²]	Cross BRAM Section [cm ²]	Cross
198	IUCF	2V1000	4.54x10 ¹³	3.21x10 ⁻¹⁴	3.52 x10 ⁻¹⁴	
198	IUCF	2V6000	4.54x10 ¹³	2.99x10 ⁻¹⁴	3.36 x10 ⁻¹⁴	
150	IUCF	2V1000	3.00x10 ¹¹	3.79x10 ⁻¹⁴	3.79 x10 ⁻¹⁴	
150	IUCF	2V6000	5.00x10 ¹¹	3.31 x10 ⁻¹⁴	3.76 x10 ⁻¹⁴	
104	IUCF	2V1000	6.01x10 ¹¹	3.75 x10 ⁻¹⁴	4.09 x10 ⁻¹⁴	
104	IUCF	2V6000	9.41x10 ¹¹	3.03 x10 ⁻¹⁴	3.47 x10 ⁻¹⁴	
74	IUCF	2V1000	1.60x10 ¹²	3.60 x10 ⁻¹⁴	3.95 x10 ⁻¹⁴	
74	IUCF	2V6000	1.00x10 ¹²	2.83 x10 ⁻¹⁴	3.21 x10 ⁻¹⁴	
40	LBL	2V1000	1.25x10 ¹²	4.20 x10 ⁻¹⁴	4.76 x10 ⁻¹⁴	
20	LBL	2V1000	4.64x10 ¹²	1.75 x10 ⁻¹⁴	1.96 x10 ⁻¹⁴	
14.9	UCD	2V1000	6.34x10 ¹²	3.65 x10 ⁻¹⁴	3.96 x10 ⁻¹⁴	
12	LBL	2V1000	4.15x10 ¹²	6.47 x10 ⁻¹⁵	6.57 x10 ⁻¹⁵	
11.73	UCD	2V1000	9.01x10 ¹²	2.82 x10 ⁻¹⁴	2.98 x10 ⁻¹⁴	
8.8	UCD	2V1000	2.40x10 ¹²	7.22 x10 ⁻¹⁵	4.74 x10 ⁻¹⁵	
8.7	UCD	2V6000	7.46x10 ¹²	7.30 x10 ⁻¹⁵	5.79 x10 ⁻¹⁵	
6.8	UCD	2V1000	1.73x10 ¹³	9.73 x10 ⁻¹⁵	8.35 x10 ⁻¹⁵	
5.3	UCD	2V1000	1.50x10 ¹¹	1.40 x10 ⁻¹⁴	1.25 x10 ⁻¹⁴	
3.8	UCD	2V1000	1.15x10 ¹²	9.10 x10 ⁻¹⁵	7.41 x10 ⁻¹⁵	

Table 8 gives the parameters selected to fit the data in accordance to the Weibull model (note the substitution of proton energy for LET).

Table 8: Proton Weibull Parameters

Parameters	Limit	Onset	Width	Power
Cells	Cm²	MeV	-	-
Config	3.8E-14	3.0	12	0.5
BRAM	4.1E-14	3.0	12	0.6
POR	3.74E-13	7.0	12	1.0
SMAP	5.72E-13	6.5	12	0.5
JCFG	2.86E-13	6.0	12	0.5

Data points obtained while using high dosed parts (higher than 400 Krad) and non-etched parts for energies below 40 MeV have been discarded from the data set considered to represent the device's proton SEU response. Test runs conducted up to total ionizing dose accumulations of ~2 Mrad demonstrated that the SEU saturation cross sections began increasing with accumulated dose above 400krad. Since the device has a TID rating of 200 krad(Si), these data points were considered inappropriate. Additionally, measurements taken on non-etched parts below 40 MeV have not been taken in account because of the uncertainty of the actual energies after penetrating the packaging material.

The circuit's sensitivities to SEUs and SEFIs are displayed in figures 11, 12, 13, 14 and 15. SEFIs started to be detected on the Virtex-II configuration memory and the block memory cells at an energy of 6.8 MeV. The saturation cross section of the configuration memory cells was found to be approximately $3.8 \cdot 10^{-14} \text{ cm}^2/\text{bit}$, while for the block RAM cells, it was $4.1 \cdot 10^{-14} \text{ cm}^2/\text{bit}$. Note that the graphs, displayed on the figures 11 and 12, prove once again that the 2V6000 is less sensitive than the 2V1000.

The SEFI curves were fit in accordance to weighted averages and statistical significance of the collected data points. In each case, the saturation cross sections are mostly driven by the highest energies because these data points have greater statistical significance (about an order of magnitude). Because these SEFI conditions have such low cross sections, the accumulated dose during testing is prohibitive to low energy proton testing. More than 30 test units were used to obtain the lower energy data set. Yet this was an insufficient number in order to obtain sufficient events for an accurate curve fit below 90% saturation.

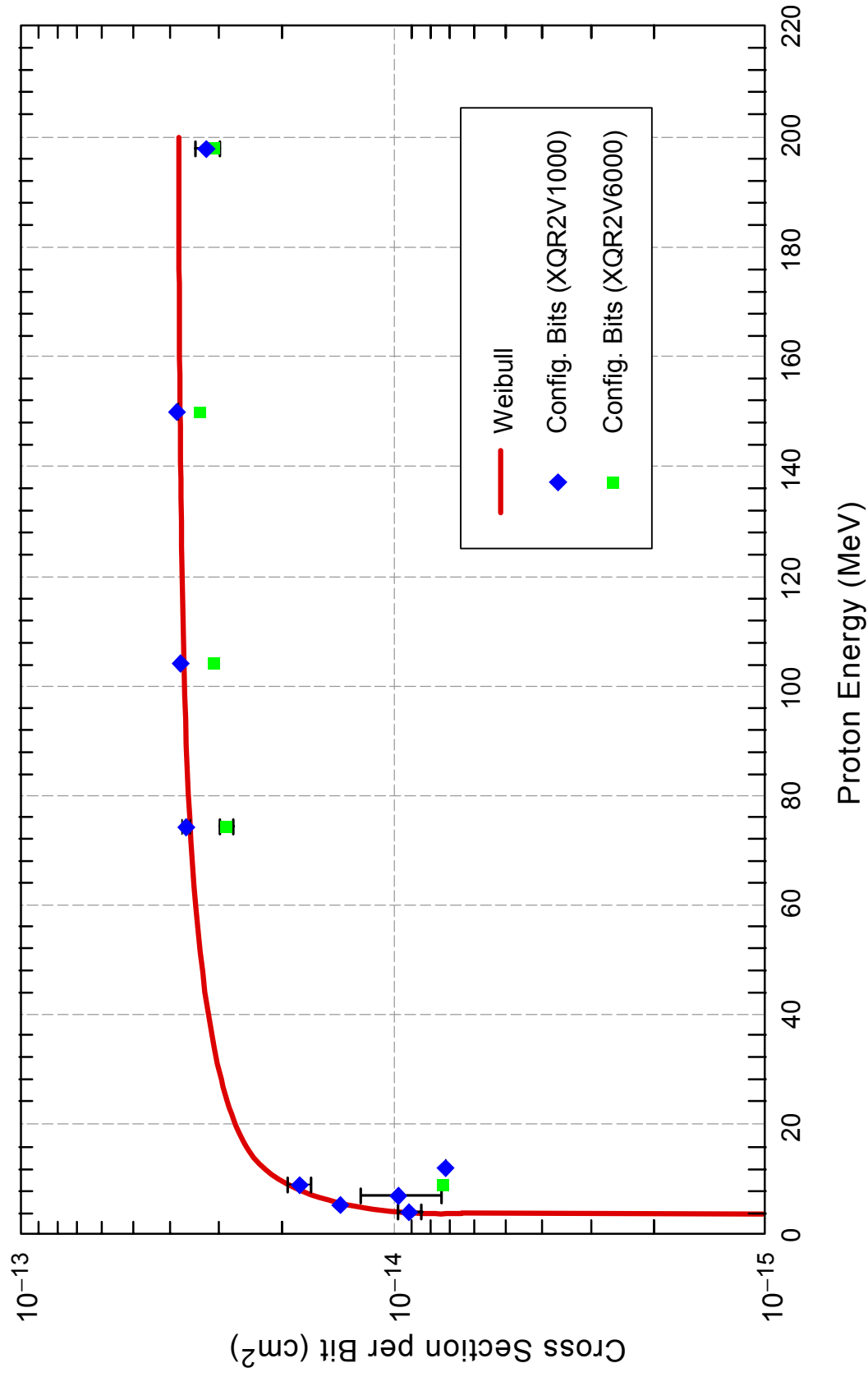


Figure 11. Virtex-II Configuration Cells
Proton SEU Cross Sections for the X-2V1000 and X-2V6000

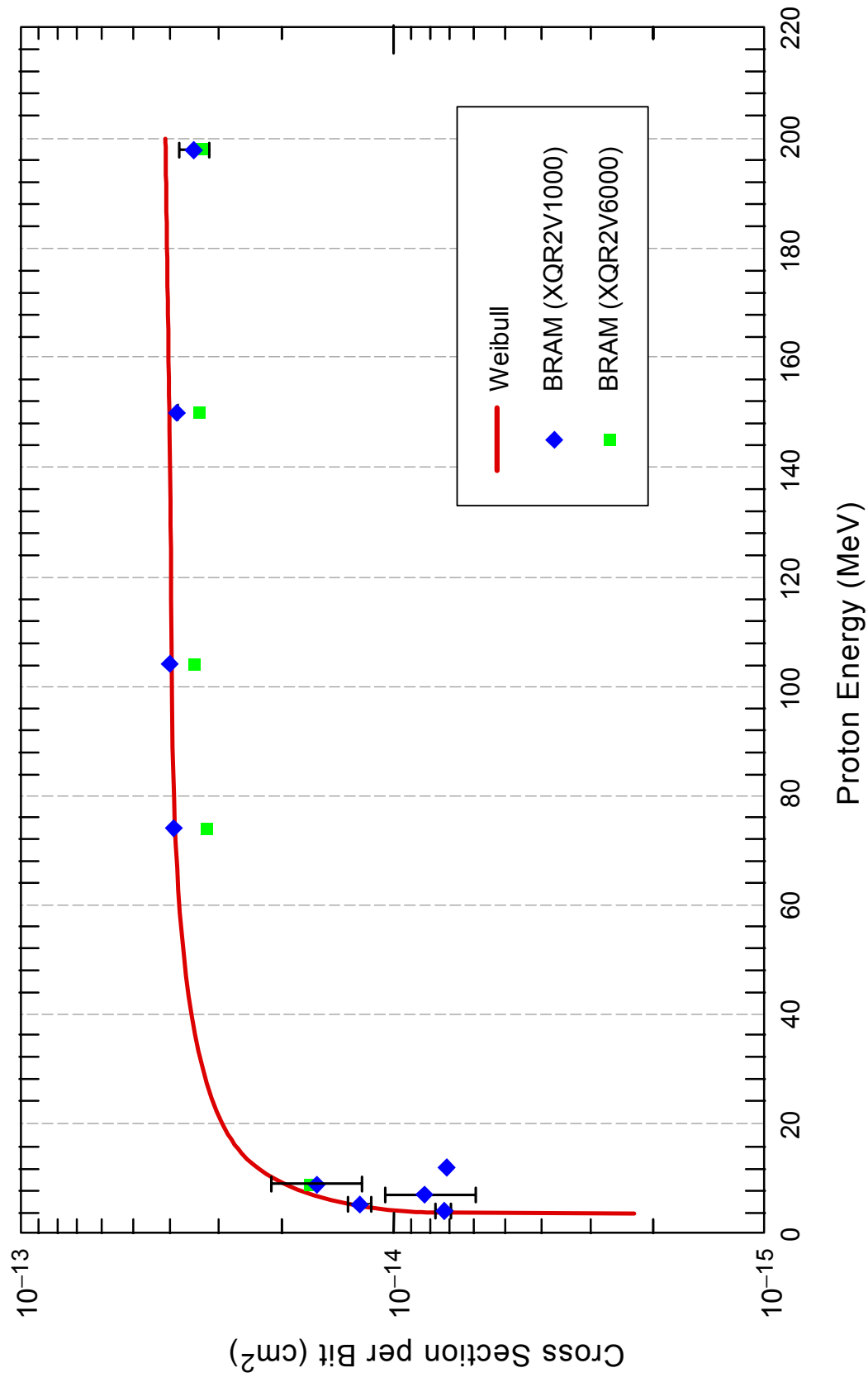


Figure 12. Virtex-II Block Memory Cells
Proton SEU Cross Sections for the X-2V1000 and X-2V6000

Table 9: Measured SEFI Cross Sections Protons' Beams

Energy [MeV]	Facility	Exposed Part Virtex-II-	Fluence [particles/cm ²]	POR Cross Section [cm ²]	SEFI Cross Section [cm ²]	SEFI Cross Section [cm ²]	SEFI Cross Section [cm ²]
198	IUCF	2V1000	4.40x10 ¹³	3.6x10 ⁻¹³	5.5x10 ⁻¹³	2.7x10 ⁻¹³	
150	IUCF	2V1000	8.00x10 ¹¹	*	1.3x10 ⁻¹²	*	
104	IUCF	2V1000	1.54x10 ¹²	*	6.5x10 ⁻¹³	6.5x10 ⁻¹³	
74	IUCF	2V1000	2.60x10 ¹²	*	7.7x10 ⁻¹³	3.8x10 ⁻¹³	
40	LBL	2V1000	1.25x10 ¹²	8.0x10 ⁻¹³	1.6x10 ⁻¹²	8.0x10 ⁻¹³	
20	LBL	2V1000	4.64x10 ¹²	2.2x10 ⁻¹³	*	*	
14.9	UCD	2V1000	6.34x10 ¹²	3.1x10 ⁻¹³	*	*	
11.73	UCD	2V1000	1.27x10 ¹³	7.9x10 ⁻¹⁴	3.9x10 ⁻¹³	1.6x10 ⁻¹³	
8.8	UCD	2V1000	9.86x10 ¹²	2.0x10 ⁻¹³	3.04x10 ⁻¹³	1.0x10 ⁻¹³	
6.8	UCD	2V1000	1.73x10 ¹³	*	1.2x10 ⁻¹³	5.8x10 ⁻¹⁴	
3.8	UCD	2V1000	1.15x10 ¹²	*	*	*	

* none observed for the given fluence

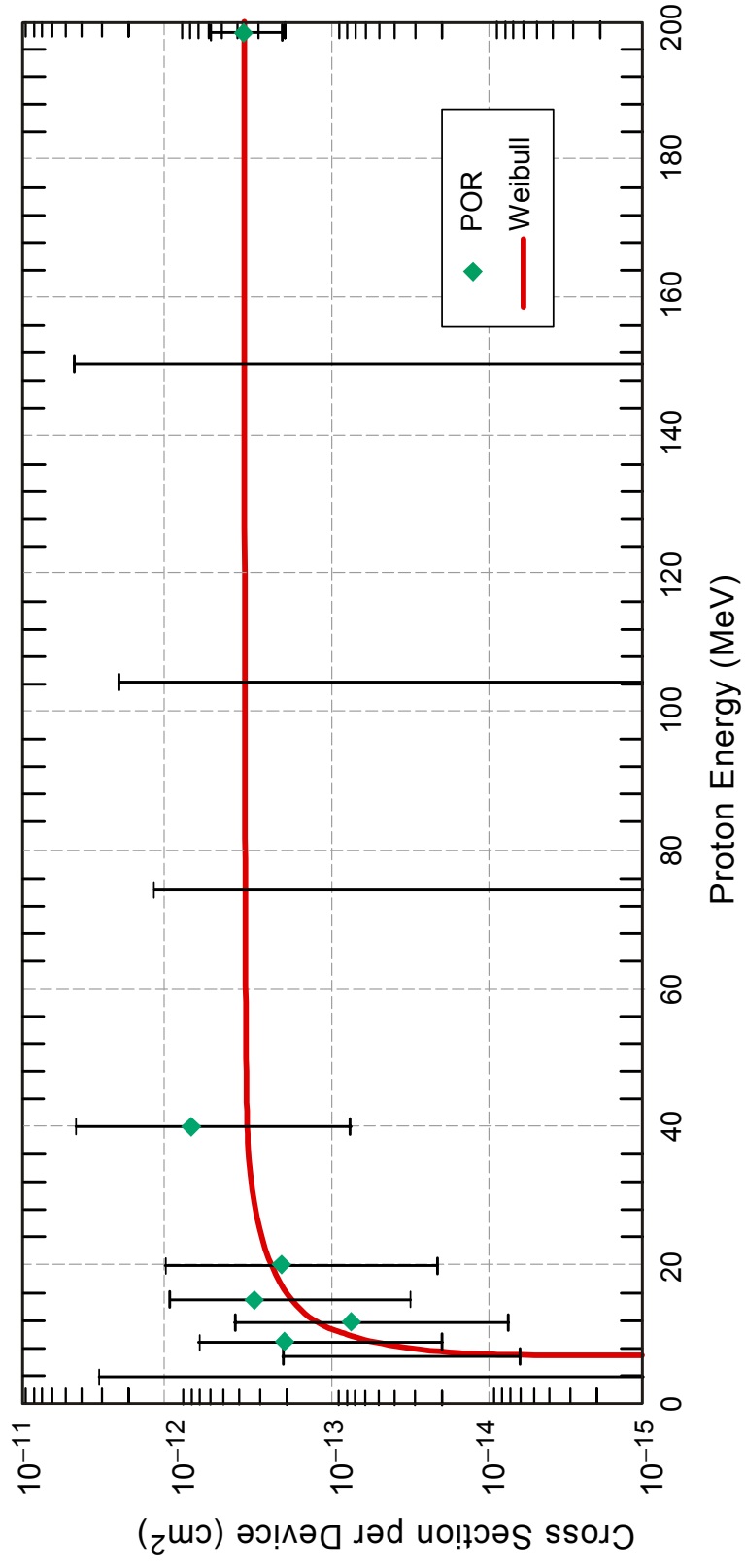


Figure 13. Virtex-II POR SEFI Cross Section

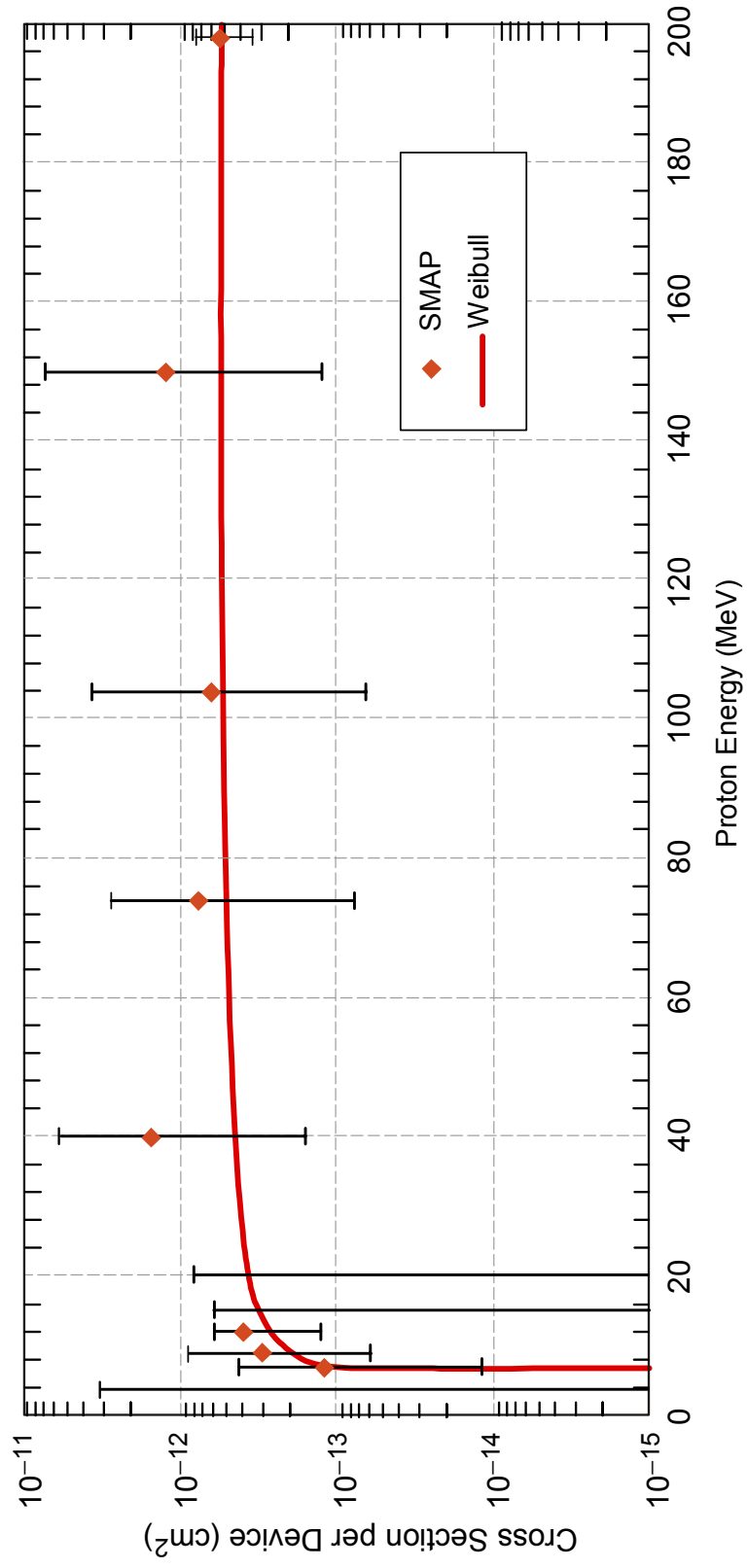


Figure 14. Virtex-II SMAP SEFI Cross Section

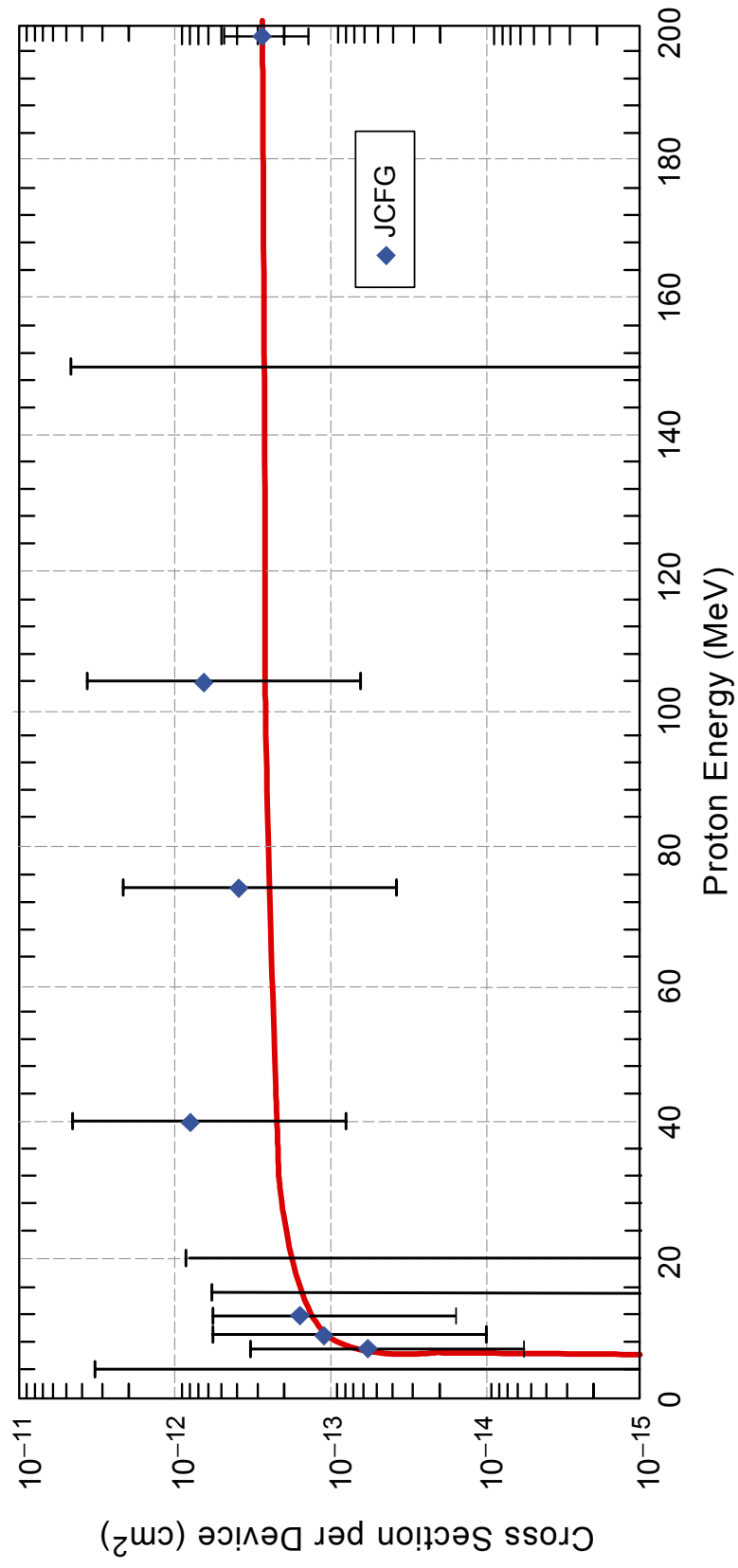


Figure 15. Virtex-II JCFCG SEFI Cross Section

VI. CONCLUSION AND FUTURE WORK

The studies performed on the Virtex-II FPGA have culminated in three publications, and have been presented in international conferences. The first two have been presented by JPL at MAPLD¹ (Military and Aerospace Programmable Logic Devices) in 2002 and at NSREC² (Nuclear and Space Radiation Effects Conference) in 2003. The Aerospace Corporation presented the third at RADECS³ (RADiation and its Effect on Components and Systems), in 2003.

Static test results performed over the year 2002, on the configuration memory of the Virtex-II XC2V1000 along with projected upset rates have been reported in a poster at MAPLD 2002 [1]. The NSREC 2003 Data Workshop paper summarizes dynamic testing experiments of the 2V1000 configuration memory cells that have been developed by Xilinx and JPL. Results demonstrate the effectiveness of mitigation techniques such as triple module redundancy (TMR) and partial reconfiguration when used in combination for the Virtex-II-1000. A comparison of the frequency of functional failures shows that simple shift register designs utilizing mitigation techniques such as partial reconfiguration or TMR alone have only a slight advantage over a non-mitigated design. However, when both methods are used, the design was observed to be essentially immune to functional errors. Those initial results on a simple test design are encouraging and suggest that using TMR and partial reconfiguration mitigation methods together can make the Virtex-II suitable for space flight applications [2]. More testing is needed on designs of greater complexity to confirm that this result is applicable and comparable with the presented results.

Additional studies have been performed by The Aerospace Corporation for the data analysis of the Virtex-II. SEE sensitivities to proton beams of the configuration, block RAM and flip-flops cells were compared with those measured with the heavy ions, using existing models. Obtained data are reported in a poster presentation at RADECS 2003 [3].

An ongoing effort for the dynamic testing of the 2V6000, taking in account the recommendations of the consortium members, has led to the design of a new specific

¹ The MAPLD conference focuses on programmable devices and technologies, as well as digital engineering and related fields geared towards military and aerospace applications.

² The NSREC conference targets the effects of space or nuclear radiation on electronic or photonic devices, circuits, sensors, materials and systems, as well as techniques for producing radiation-tolerant devices and integrated circuits.

³ The RADECS conference promotes basic and applied scientific research principally in the area of radiation and its effects on materials, components and systems. This conference targets the space, the civil nuclear, and the military applications.

board designed and manufactured by SEAKR Inc. Its main features will be described in the next report. Further testing of the Virtex-II, based on the use of this board, in the months ahead has been scheduled to study upsets during dynamic operations of this Virtex-II device and the epitaxial version when it becomes available.

VII. REFERENCES

- [1] C. Yui, G. Swift and C. Carmichael, Single Event Upset Susceptibility Testing of the Xilinx *Virtex-II* FPGA, MAPLD 2002, Maryland, September 10-12, 2002.
- [2] C. Yui, Gary M. Swift, Carl Carmichael, Rocky Koga and Jeffrey S. George, “SEU Mitigation Testing of Xilinx Virtex-II FPGAs”, Candice Poster Session, NSREC Monterrey, 2003.
- [3] Koga R., George J., Swift G., Yui C., Carmichael C., Langley T., Murray P., Lanes K., Napier M, “Comparison of Xilinx Virtex-II FPGAs SEE sensitivities to Protons and Heavy Ions”, RADECS 2003 (RADiation and its Effect on Components and Systems), Noordwijk, The Netherlands, 15 - 19 September 2003.

APPENDIX I: THE COMPLETE DATA SET

The configuration bits and BRAM cross sections corresponding to the complete data set, obtained while performing Virtex-II radiation testing experiments, for the 2V1000 and the 2V6000, at normal incidences as well as at other incidences, are displayed in figures 16 and 17.

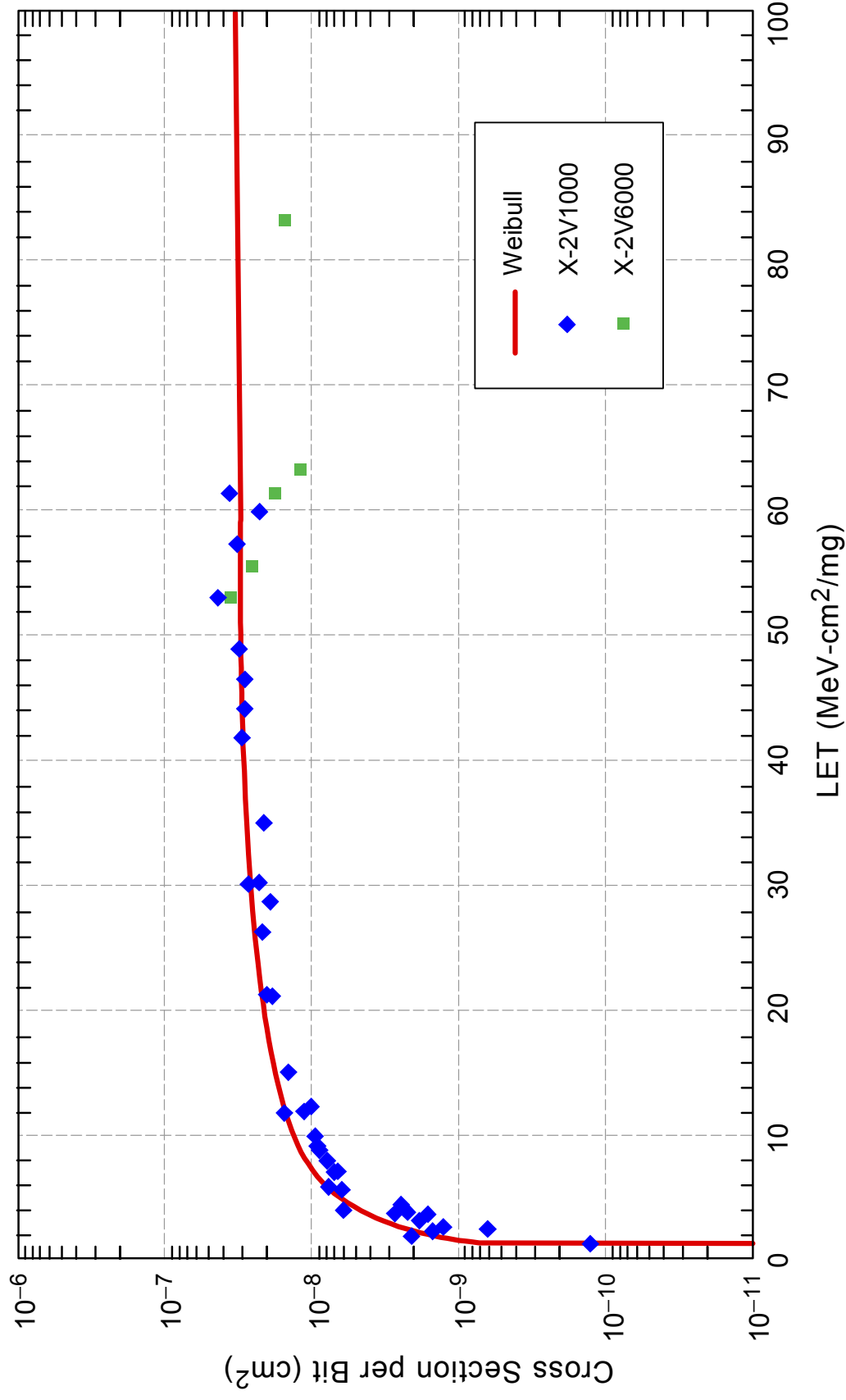


Figure 16. Virtex-II Configuration Memory Cells
Heavy Ion SEU Cross Sections for the X-2V1000 and X-2V6000 Measured at Texas A&M

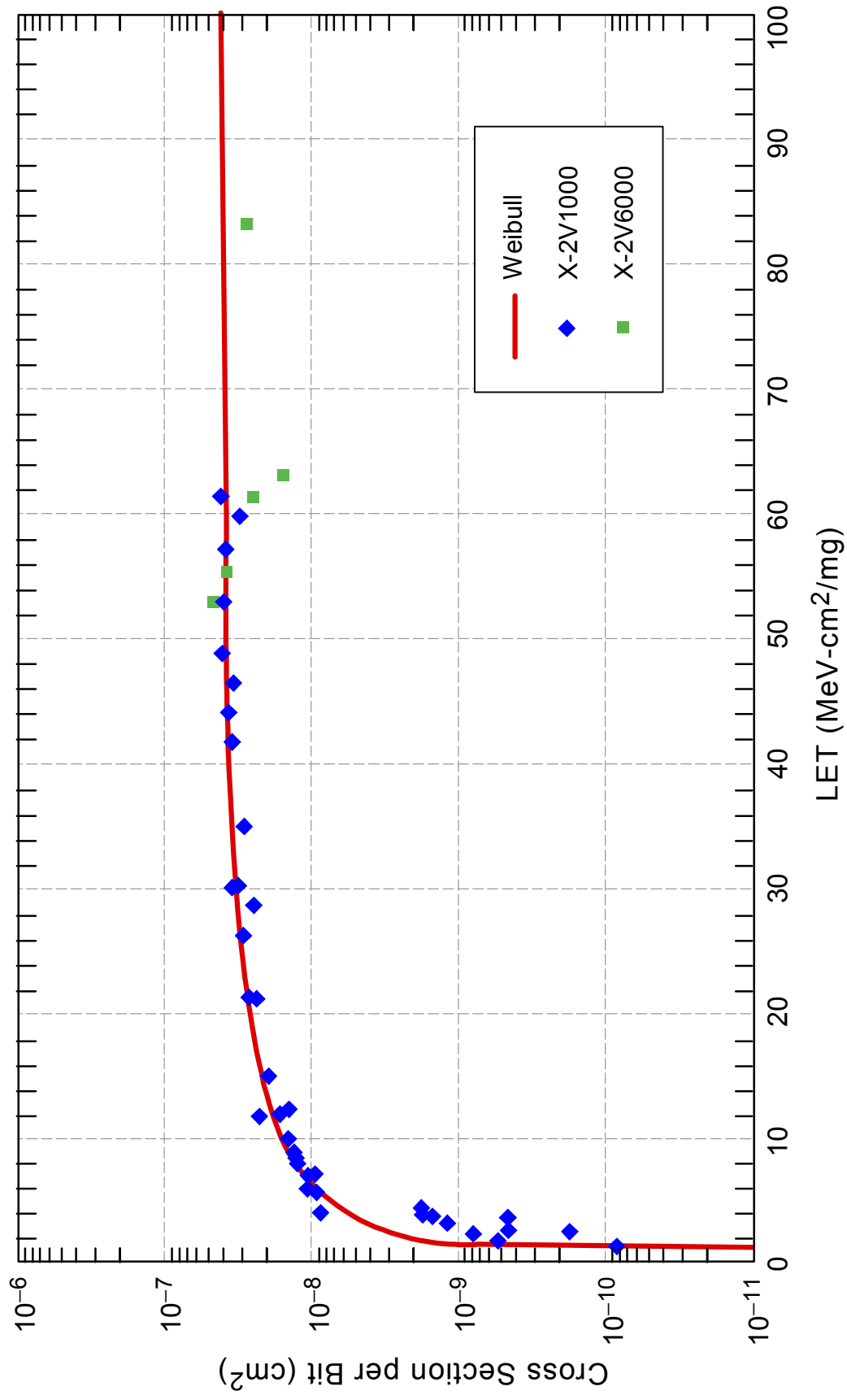


Figure 17. Virtex-II Block Memory Cells
Heavy Ion SEU Cross Sections for the X-2V1000 and X-2V6000 Measured at Texas A&M